Comparison of CPU's in FPGA's

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Agenda

- Overview
- CPU's
  - PB8051
  - Altera Nios II Gen2
  - Xilinx MicroBlaze
  - Altera Cyclone V SoC
  - Xilinx Zynq
- Benchmarks
  - Sieve of Eratosthenes
  - Dhrystone

Sensor to Image GmbH

- Company
  - Founded 1989 and privately owned
  - Team of 9 developers, 2 people in production and 3 in administration
  - Company goal: development, production and service of OEM image processing hardware tool
  - Full service from training → development → layout → software → sample production → redesign → series production → support → repair is possible
  - Production of 1000-2000 boards/year
- Development
  - High speed and impedance controlled layout, ptich > 0.8 mm
  - FPGA design tools experience with Altera, Xilinx, Lattice and MicroSemi tools
  - FPGA simulation and verification with ModelSim 10.x
  - Embedded C-Compilers for FPGA based 8051, Coldfire, MicroBlaze/NIOS, ARM in Zynq/Cyclone V SoC and BLACKFIN running Linux
  - Capability for writing PC drivers VC6 – VC2015
- Production
  - Semiautomatic Pick & Place machine with manual BGA placement and part handling down to size 0402
  - Vapor phase oven for RoHS conform soldering PCB size <= 30x30 cm
  - Thermal box for testing systems up to 50x50x50 cm under operation from -40° C up to 90° C
  - Mixed signal oscilloscopes with bandwidth of 5 GHz

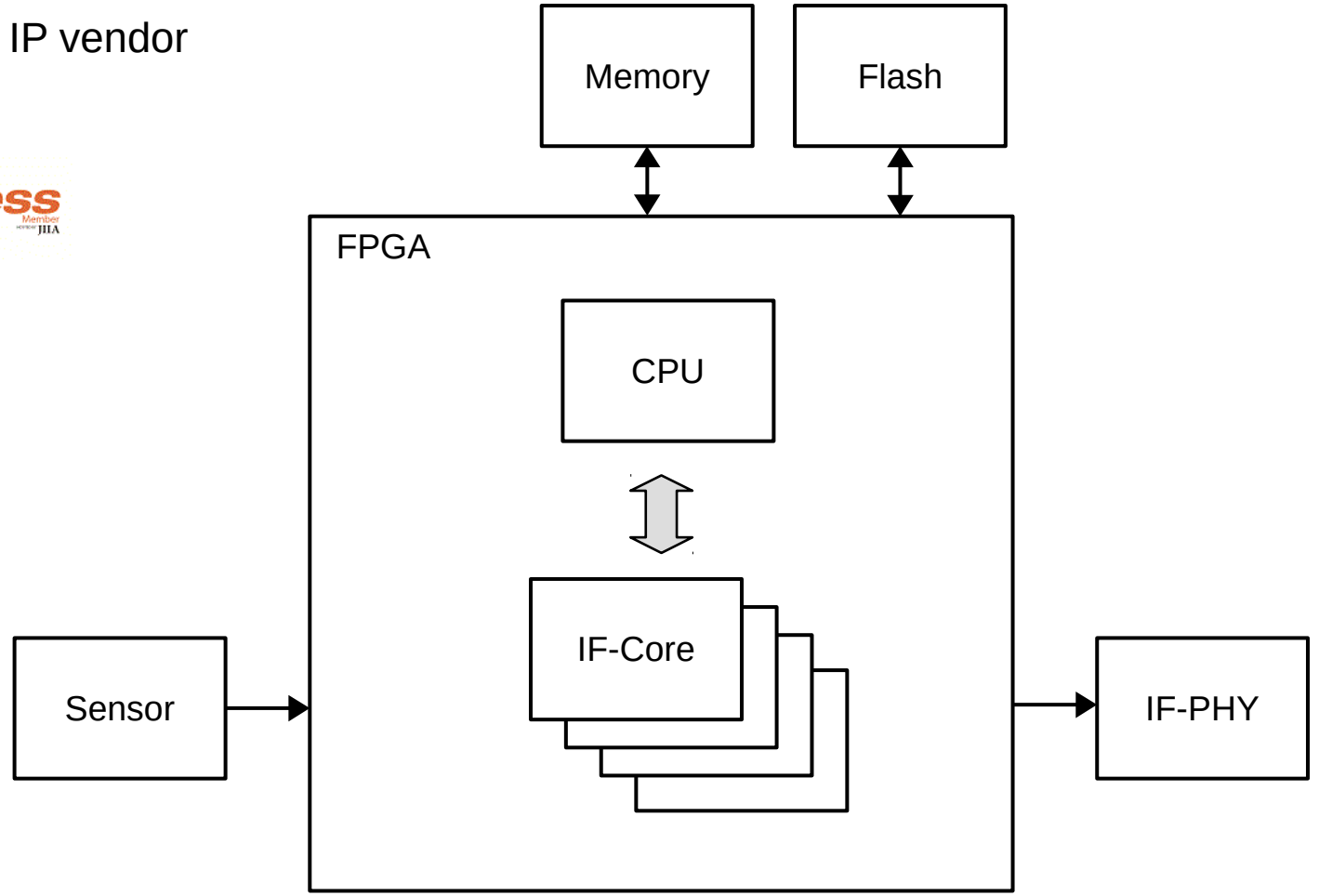
Certificated & Applications

- EN ISO9001:2008 and EN ISO 14001:2009 certified procedures since 1996
- CE Production to EN 61000-6-3:2007 and EN 61000-6-4:2007 standard
- Production to MIL-STD-810E 501.3, ...502.3, … 514.4-All, … 516.4 and VG95328, VG95373 and VG96903
- Production to Marine standard EN 60945:2002
- Asia OEM application: inspection of copper in PCB production, >= 700 PCIe line scanning systems
- German OEM application: A0 printer & scanner electronics, >= 2000 CIS & USB3 IF boards
- American OEM application: 3D OEM camera, standard CMOS Sensor FPGA pre-processing and embedded Linux, >= 1000 system
- …
- And you are welcome to verify this by yourself by visiting us in Schongau

Typical S2I FPGA system

- Machine Vision FPGA IP vendor

- FPGA's:
  - Altera
  - Xilinx
  - Lattice
  - MicroSemi
- CPU's:
  - 8051
  - Mico8/32
  - Nios II
  - MicroBlaze
  - ARM A9 (C5 SoC / Zynq)

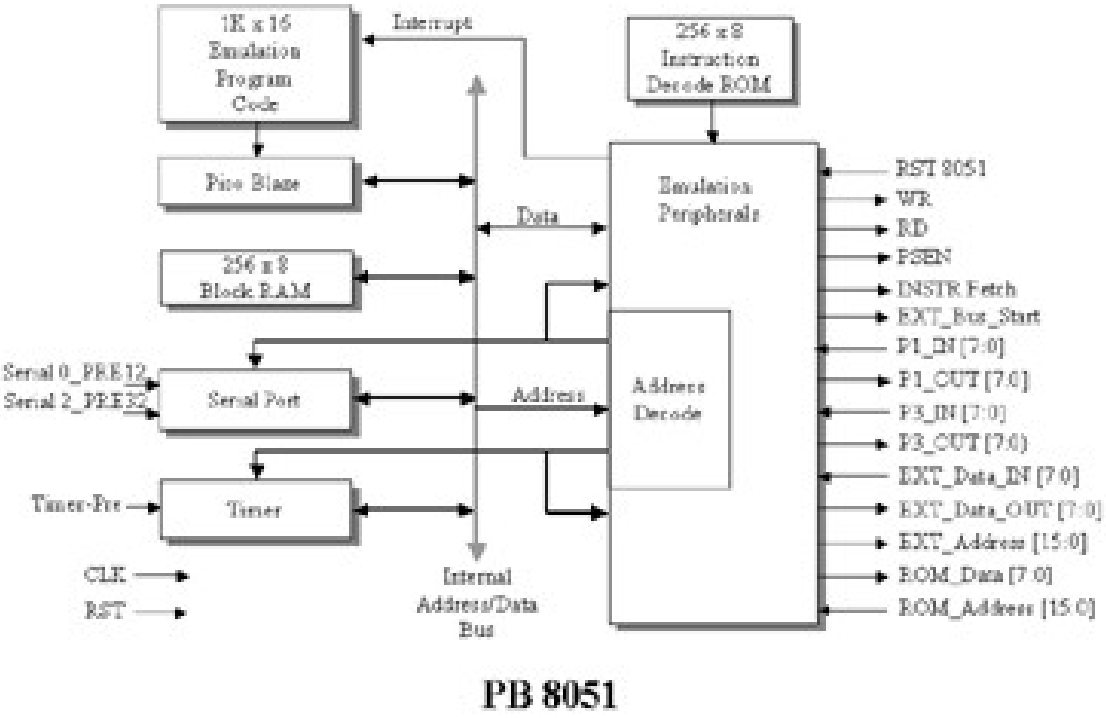


CPU's

- PB8051
- Altera Nios II Gen2
- Xilinx MicroBlaze (9.5)
- Altera Cyclone V SoC
- Xilinx Zynq 7015

PB8051

- 8-bit 8031 classic micro controller
- Build as a code interpreter to existing XILINX PicoBlaze or KCPSM6
- Not 1:1 compatible in code execution timing
- 1:1 compatible to existing compiler, OS and 8051 tools
- Can be run in different speeds to simplify clocking
- Very small, 350 slices plus BRAM for code/data
- No longer in maintenance and not tested in VIVADO

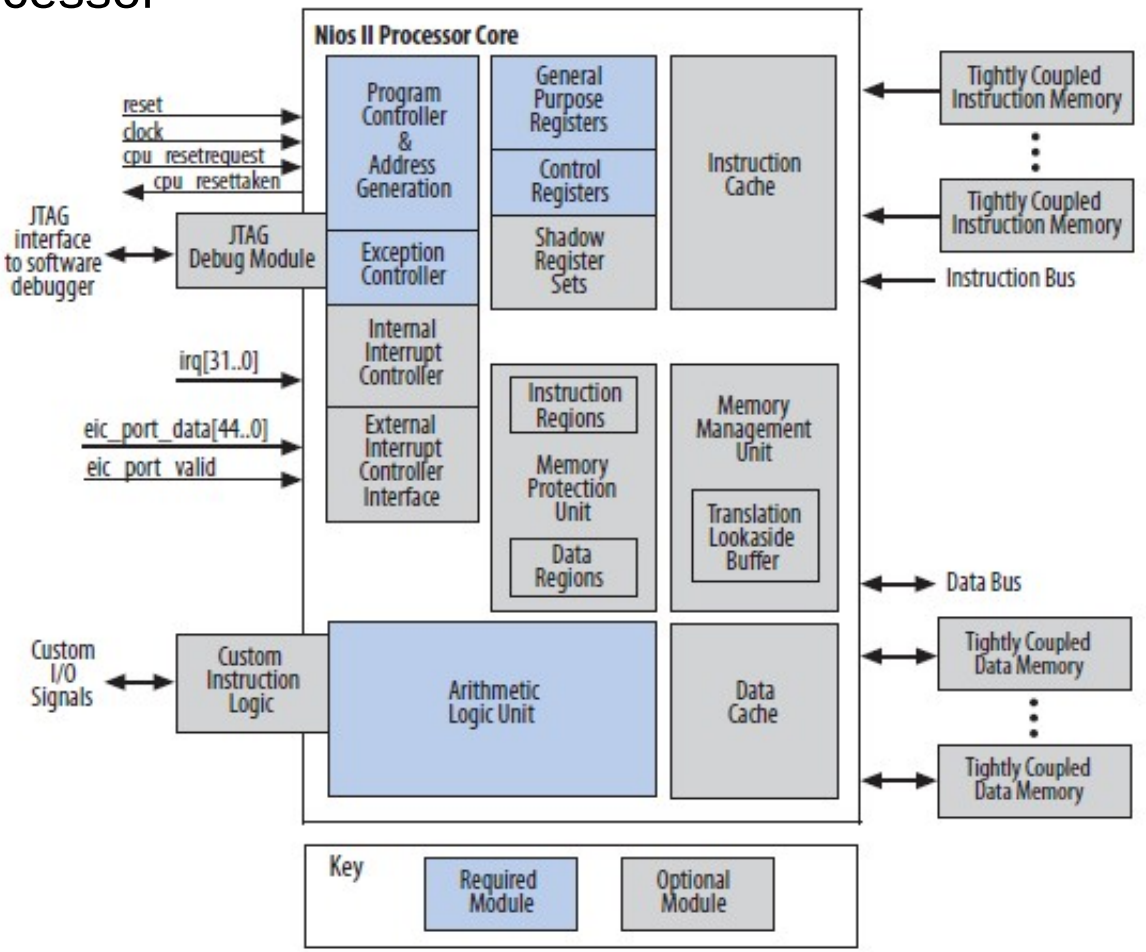


PB 8051

Altera Nios II gen2

- 32-bit RISC embedded soft processor
- Little Endianness
- Interconnect:
  - Altera Avalon
  - ARM AMBA AXI
- Highly configurable
  - Memory Management Unit
  - Memory Protection Unit
  - ...
- 2 Variants:
  - Nios II/f
  - Nios II/e

Figure 2-1: Nios II Processor Core Block Diagram



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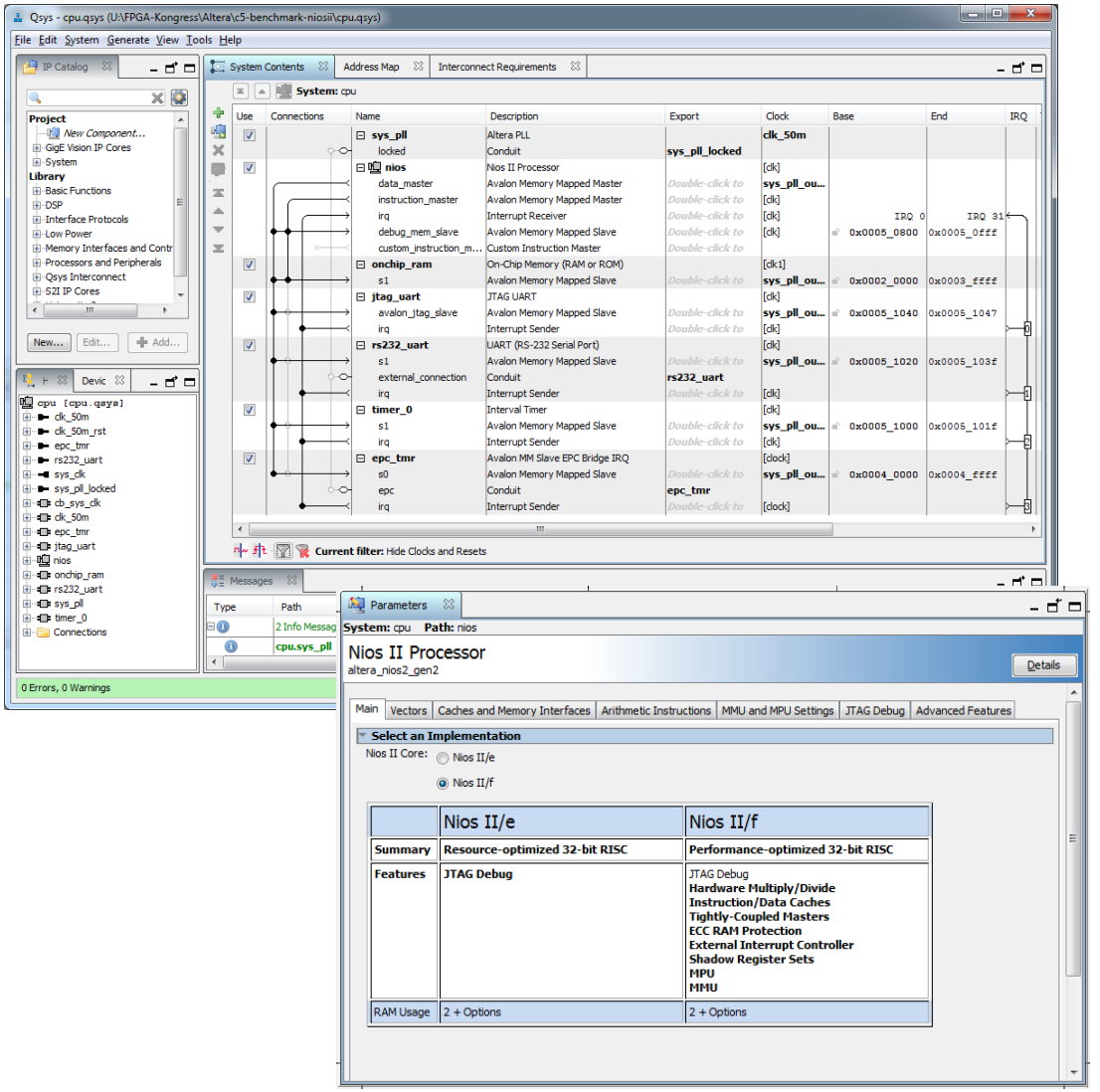
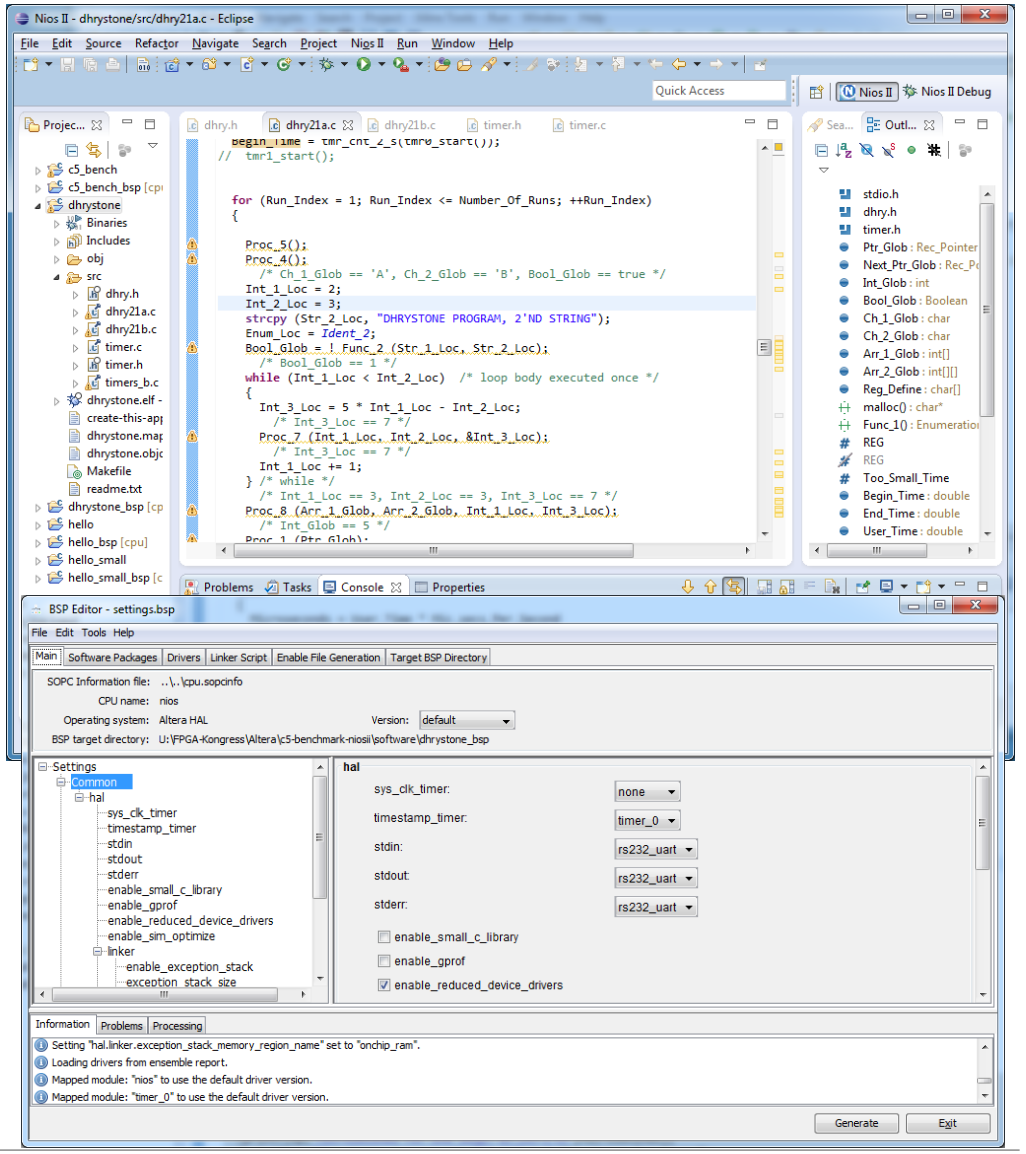
Nios II – System Design

- Qsys system integration tool
- IP Catalog
- Automatic generation of interconnect logic
- Support of Avalon, ARM AMBA AXI, AMBA APB, AMBA AHB
- Hierarchical design flow
- Automatic HDL generation



Nios II – SW Development

- Nios II Embedded Design Suite
  - Nios II Software Build Tools for Eclipse
  - Compilers
  - Debuggers
  - Device drivers
  - Bare metal HAL
  - Nios II Command Shell
  - System Console
- <design>.sopcinfo
  - BSP generation
- system.h



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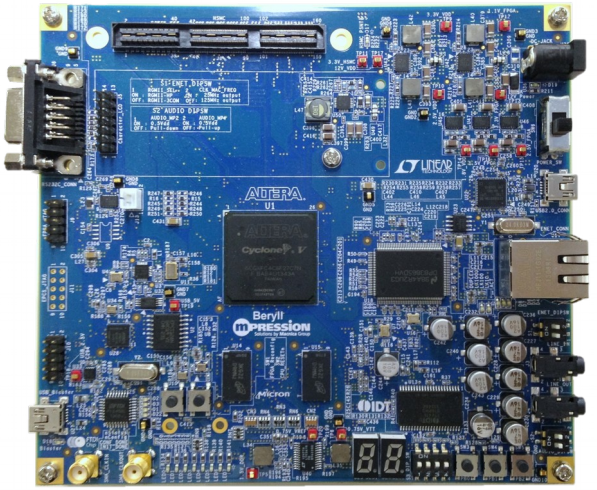
Nios II – HW Platform

- MPRESSION Beryll – Cyclone V GX Baseboard
  - FPGA: 5CGXFC4C6F27C7N
    - 50K logic elements
    - 18,868 ALM blocks
    - 6 x 3.125 Gbps transceiver
    - 70 DSP blocks
    - Memory (Kb): 2,500 M10K; 295 MLAB
- Benchmark Design
  - Logic utilization (in ALMs): 1,476 / 18,860 (8%)
  - Total RAM blocks: 128 / 250
- Nios II of Benchmark Design
  - Logic utilization (in ALMs): 842
  - Total RAM blocks: 8
  - f_max: 128 MHz



Xilinx MicroBlaze

- 32-bit RISC embedded soft processor
- Big/Little Endianness
- Interconnect:
  - PLB / LMB
  - AXI
- Highly configurable
  - Memory Management Unit
  - Floating-Point Unit
  - ...
- 6 Variants

Table A-4: **Device Utilization - Artix-7 FPGAs (XC7A200T fbg676-3)**

Configuration	Device Resources		
	LUTs	FFs	F_{max} (MHz)
Minimum Area	648	214	234
Maximum Performance	3879	3064	154
Maximum Frequency	906	545	234
Linux with MMU	3653	3218	142
Low-end Linux with MMU	3108	2582	153
Typical	2070	1777	190

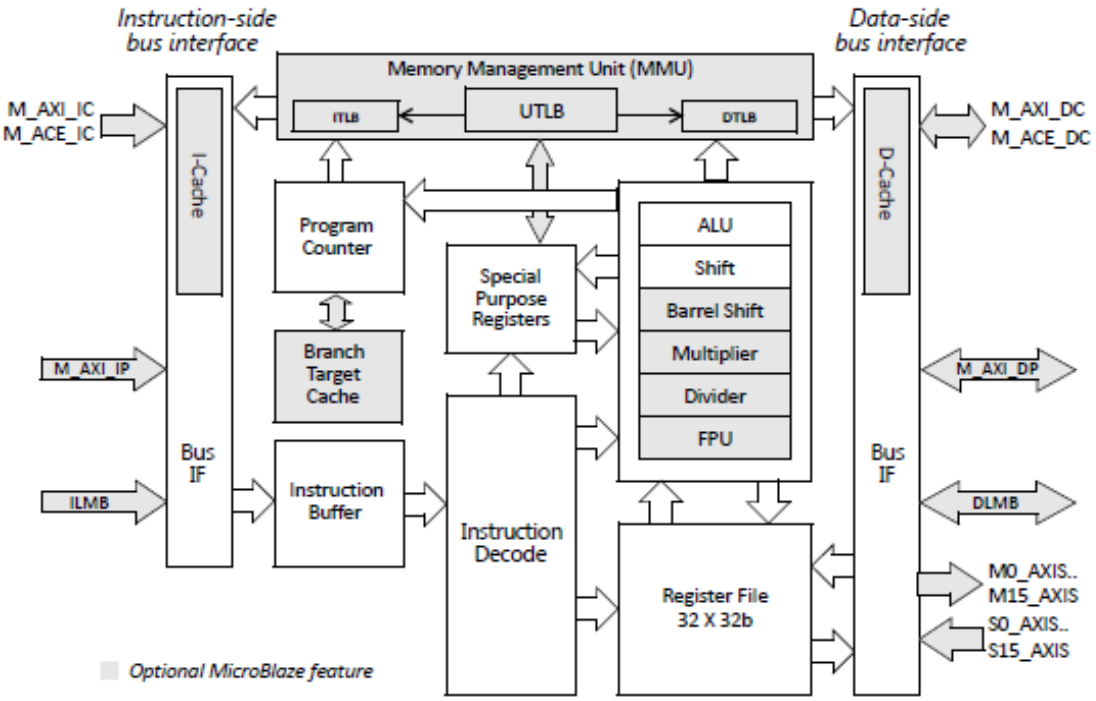


Figure 2-1: **MicroBlaze Core Block Diagram**

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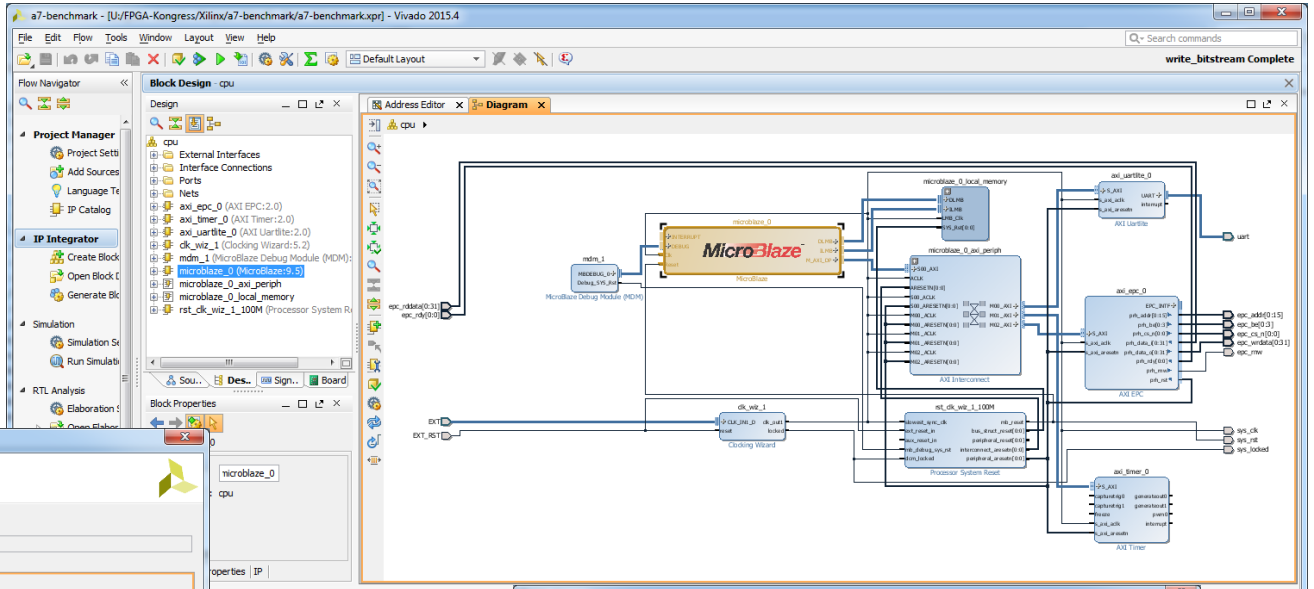
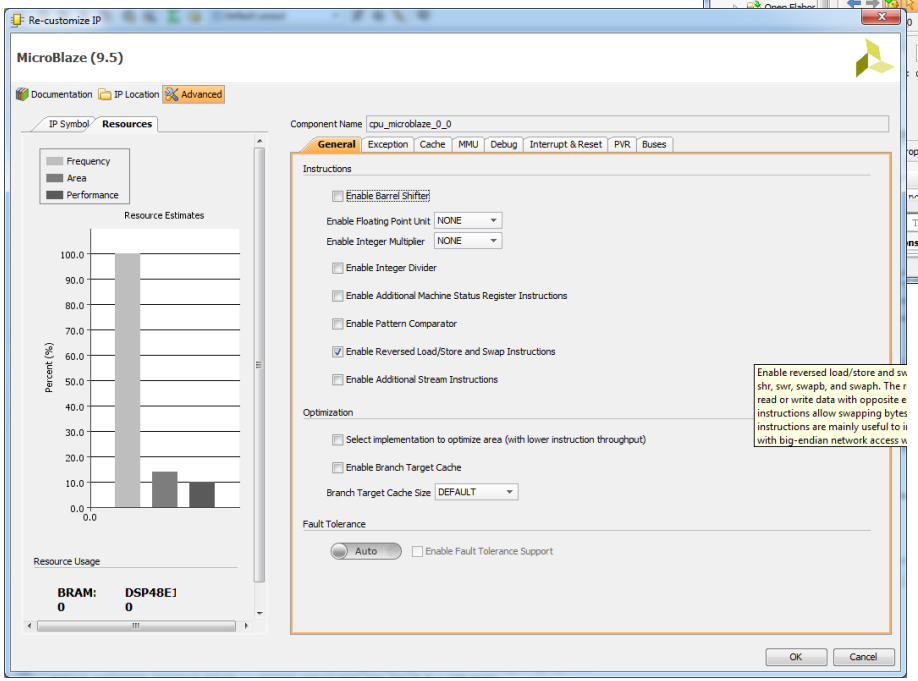
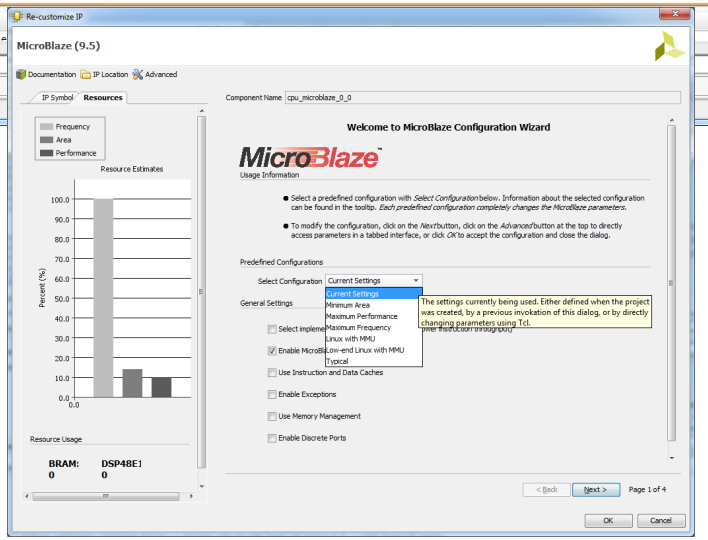
MicroBlaze – System Design

- Vivado IP Integrator
- IP Catalog
- Supports intelligent auto-connection







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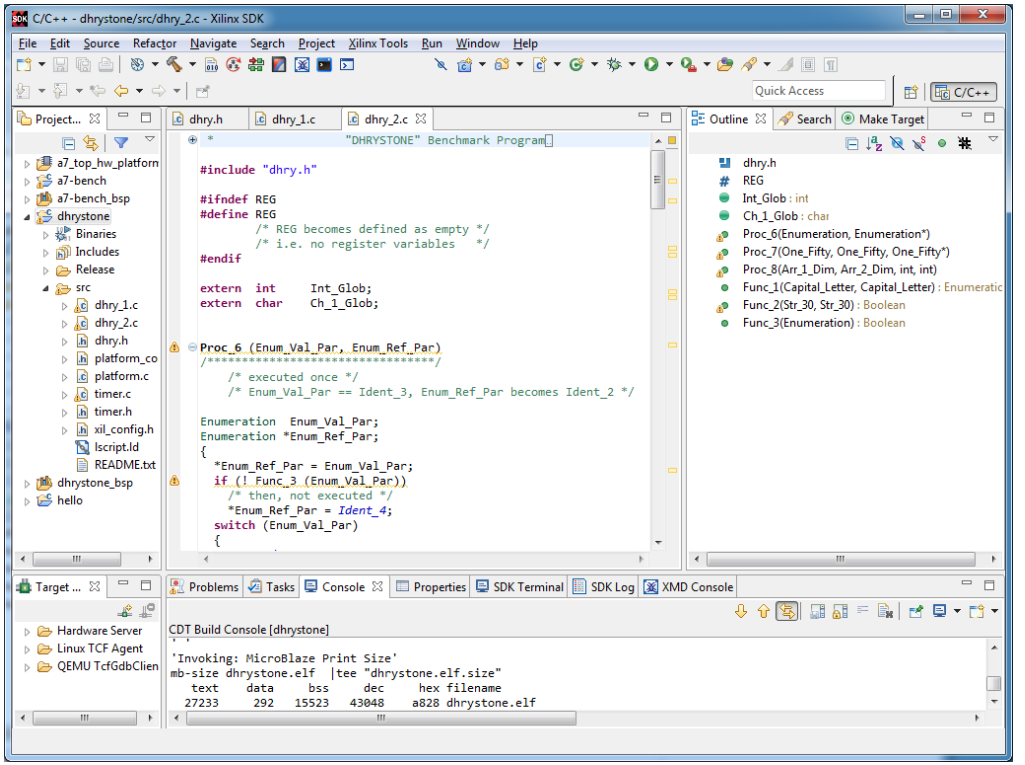
MicroBlaze – SW Development

- XSDK (Xilinx Software Development Kit)
  - Compilers
  - Debugger
  - Device drivers
  - Libraries
  - XMD Console
- <design>.hdf
  - HW platform generation
- xparameters.h



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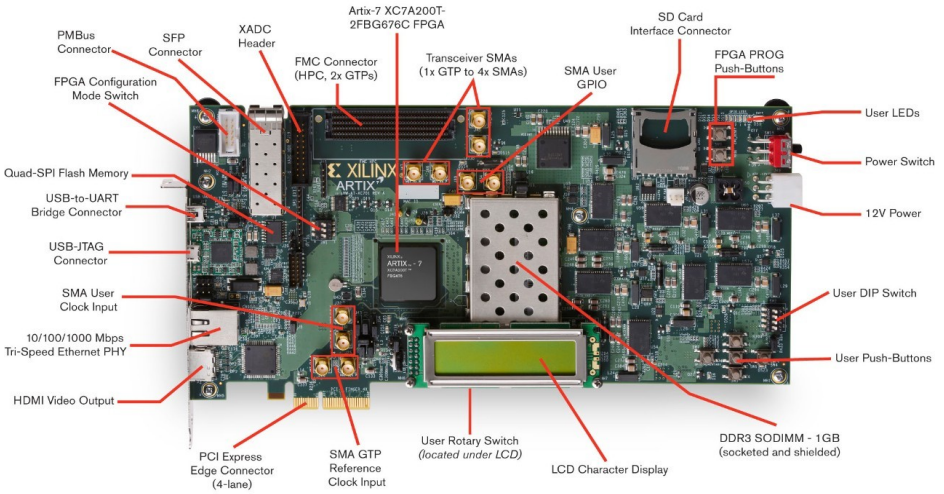
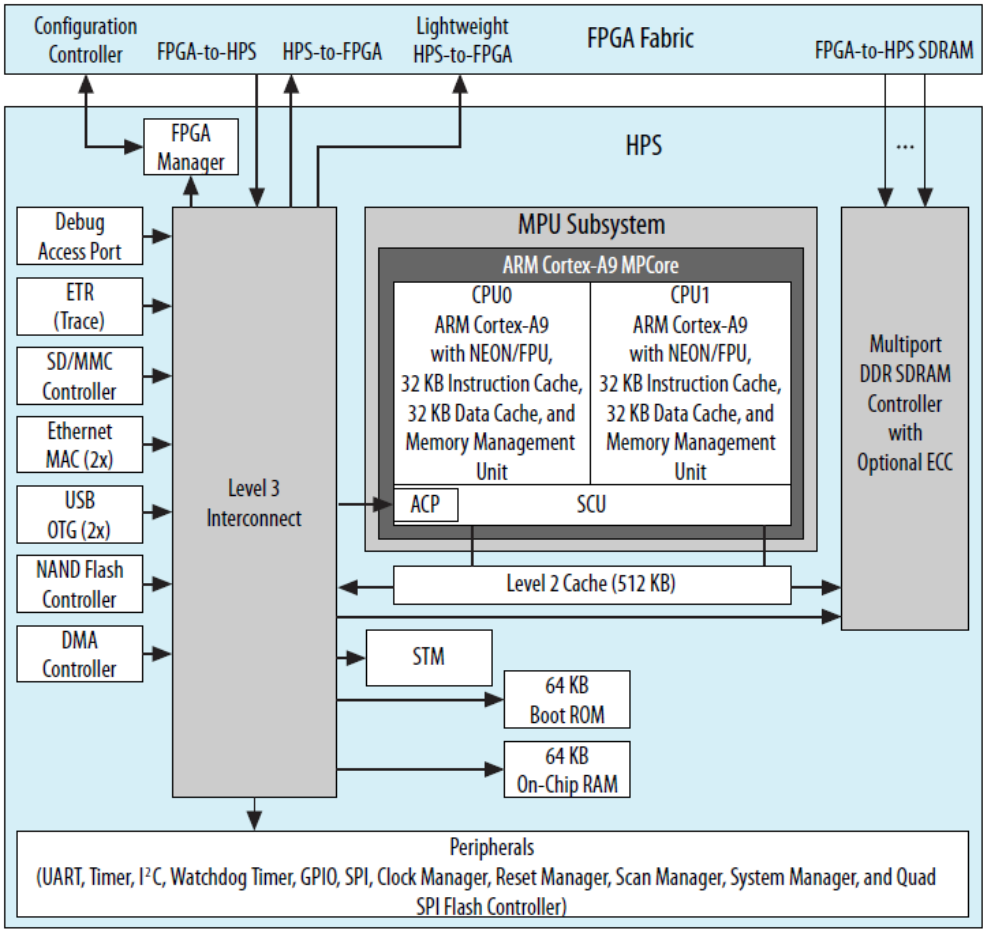
MicroBlaze – Platform

- Xilinx AC701
  - FPGA: Artix-7 XC7A200T-2FBG676C
    - 215,360 logic cells
    - 269,200 FFs
    - 740 DSP slices
    - Block RAM (Kb): 12,140
- Benchmark Design
  - Logic utilization:
    - LUTs: 1,888 / 134,600 (1.40%)
    - FFs: 1,736 / 269,200 (0.64%)
  - BRAM: 32 / 365
- Microblaze of Benchmark Design
  - LUTs: 1118
  - FFs: 926
  - f_max: 137 MHz



Cyclone V SoC

- 28 nm Low Power (28LP) process
- Hard Processor System (HPS)
  - 32 bit dual-core ARM® Cortex™-A9 MPCore
  - HPS-FPGA Bridge (Avalon, AXI3)
  - I/O peripherals
- FPGA Fabric
  - Dynamical & partial reconfiguration
  - Hard-IPs (DSP, PCIe, Memory Controller)
  - Complex logic block
  - 10 Kb Block RAM with ECC
- rocketboards.org
  - RefDesigns, tutorial, …



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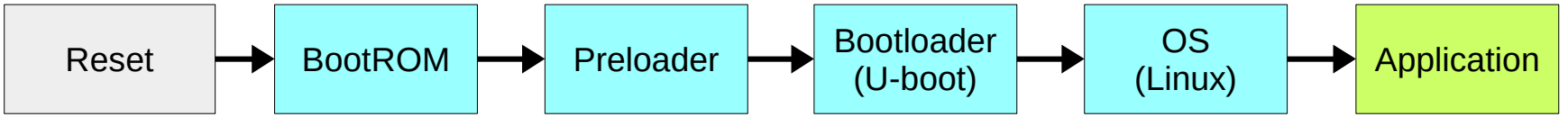
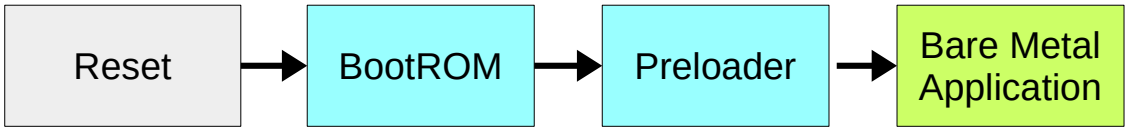
Altera SoC Boot Flow

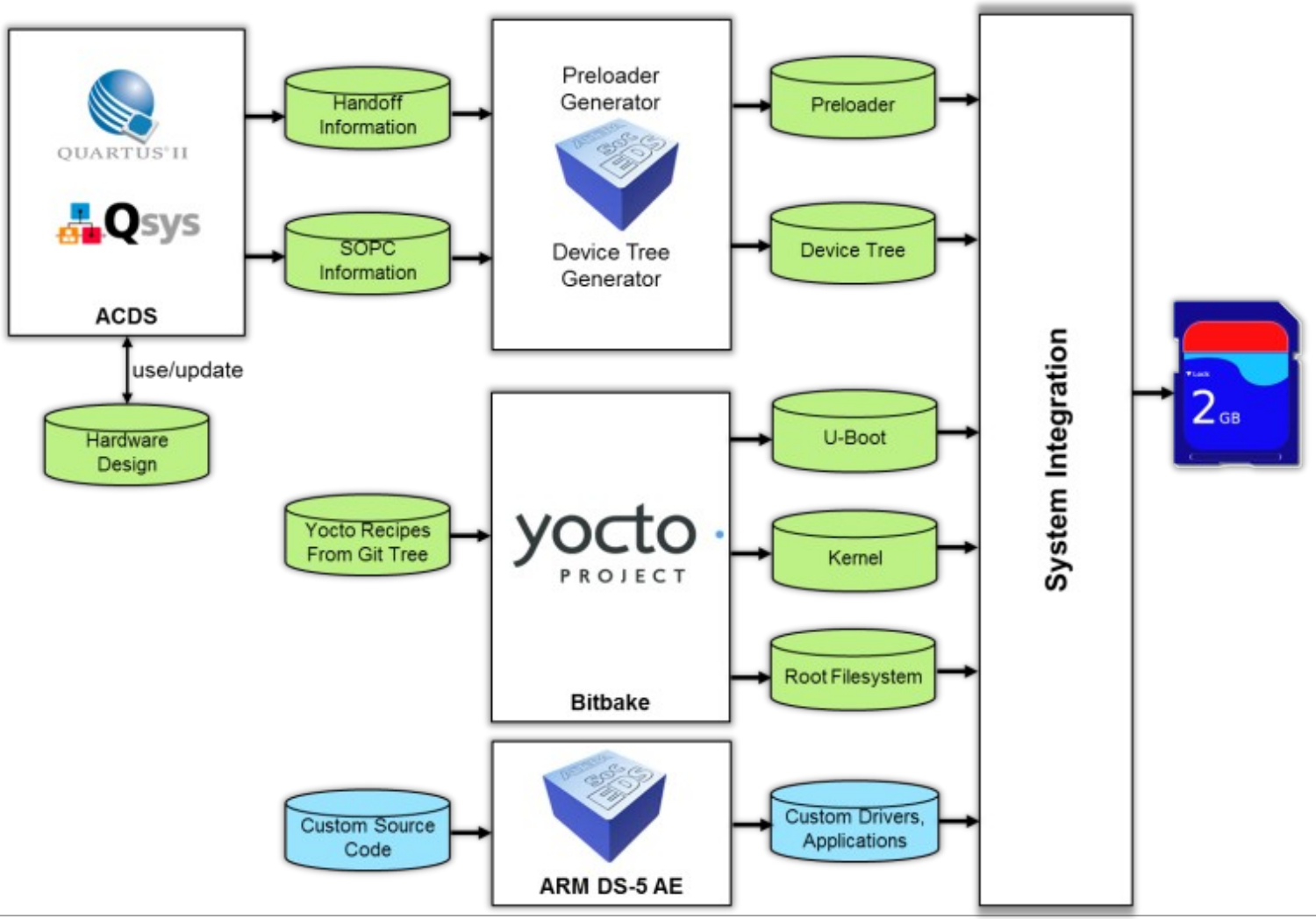
- Boot flow of typical operating system



- Boot flow of bare metal application

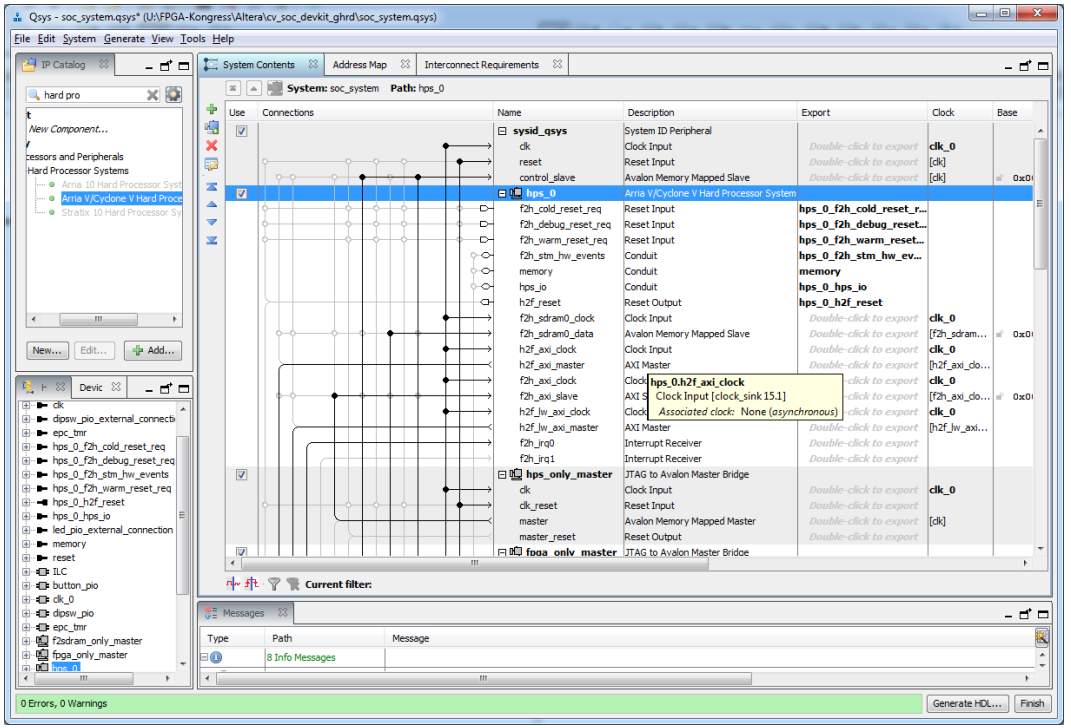


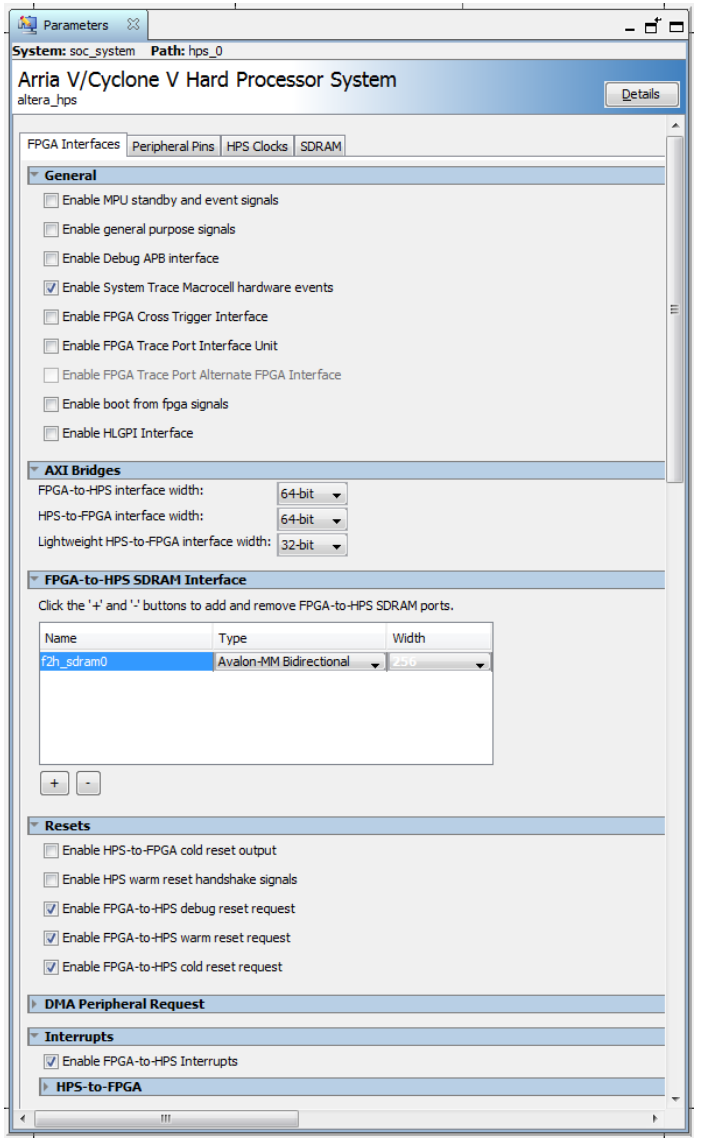
Cyclone V SoC Design Flow



Cyclone V SoC – System Design

- Tools: Quartus, Qsys





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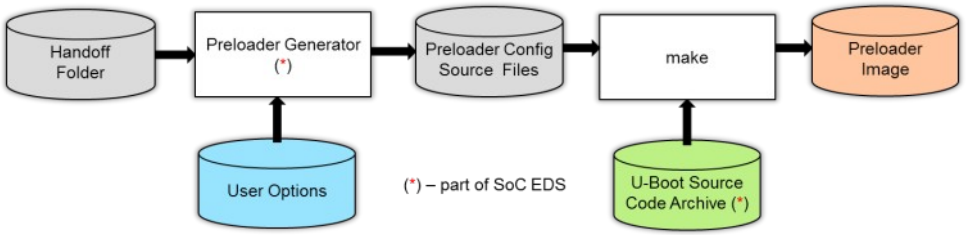
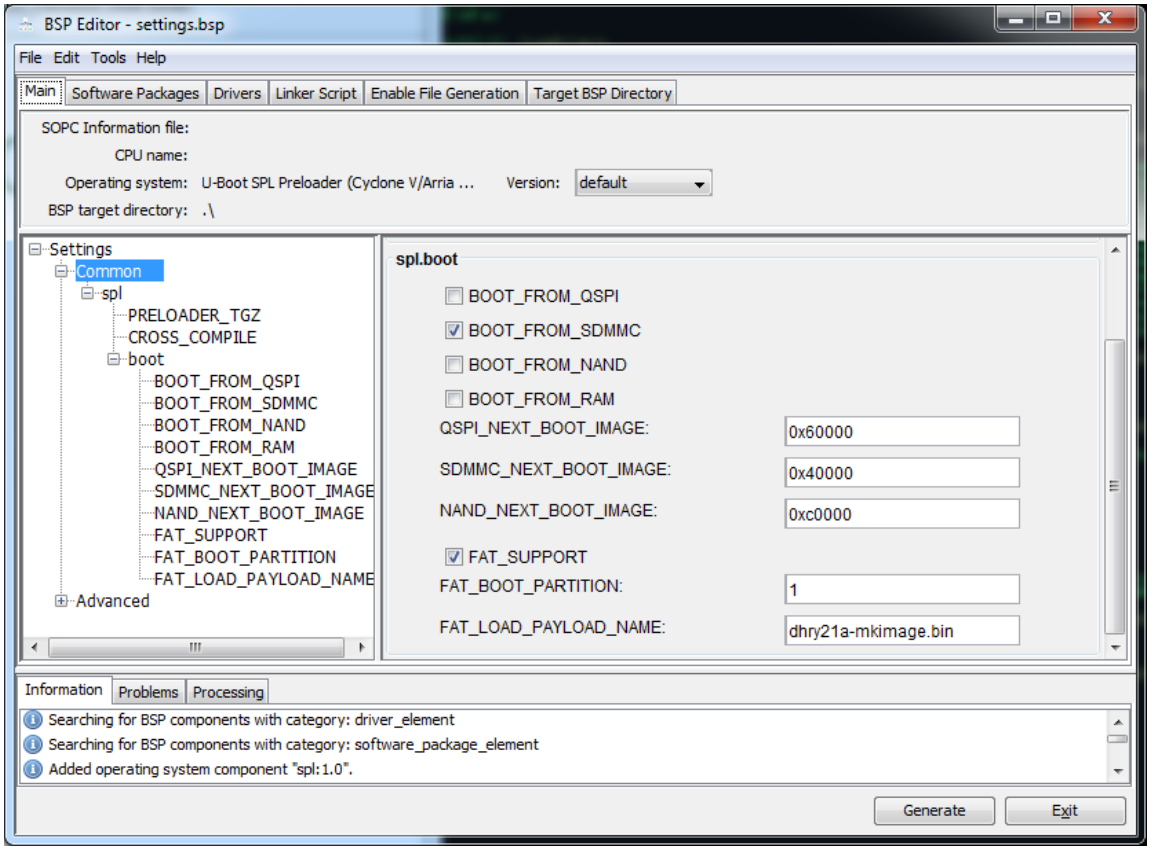
Cyclone V SoC – Preloader

- Embedded Command Shell
- Preloader Generation
  - BSP-Editor





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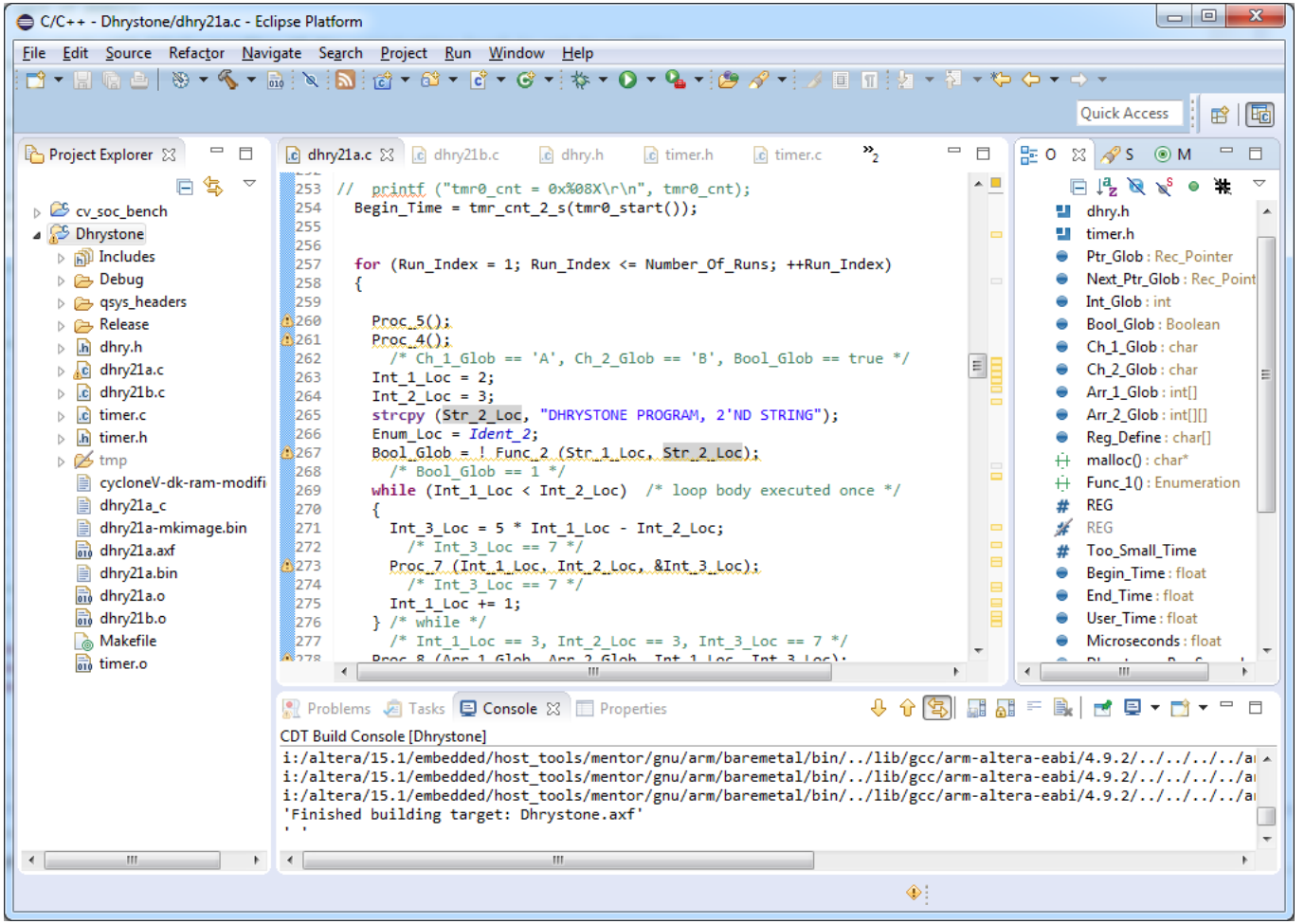
Cyclone V SoC – SW Development

- ARM DS-5 Altera Edition
  - No system.h Generate Qsys headers instead
  - Extra license needed for debugging

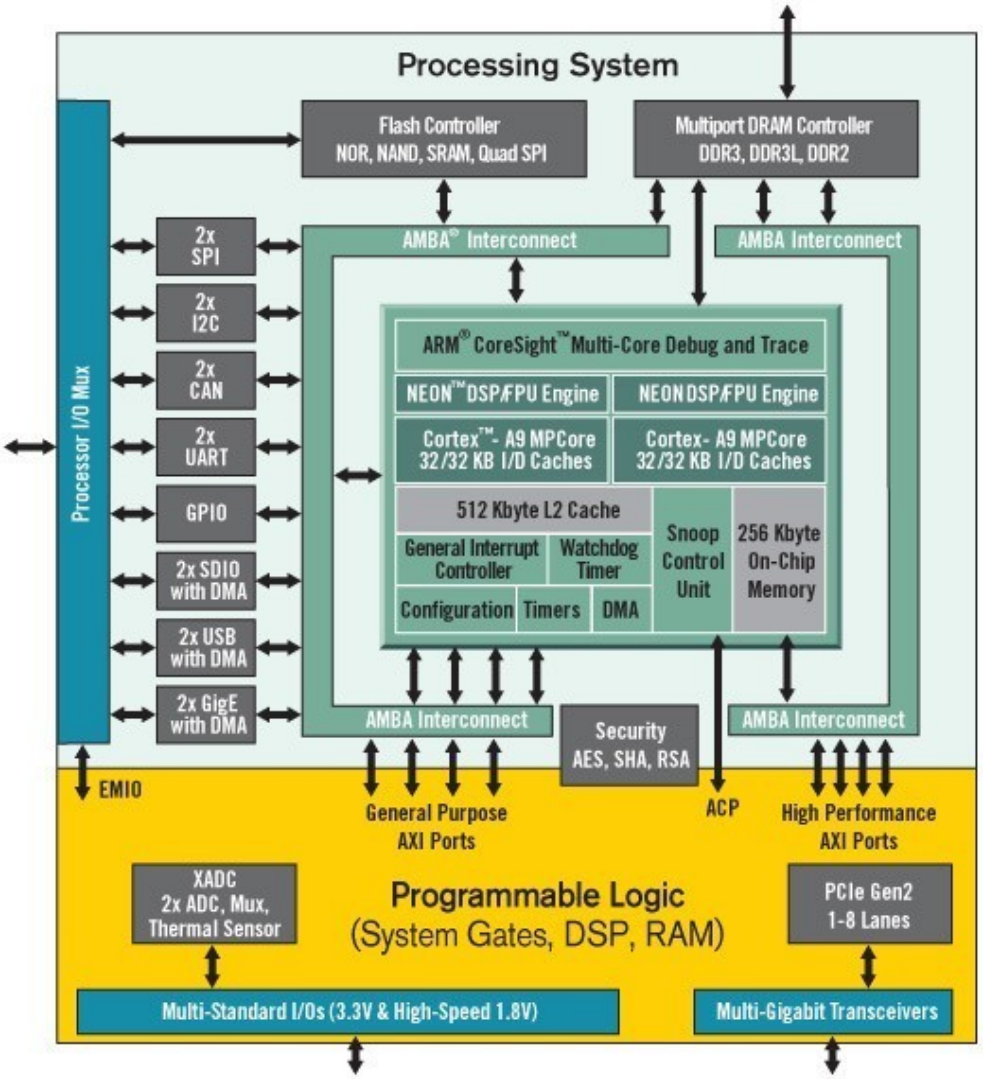


Cyclone V SoC Platform

- Cyclone V SoC Development Board
  - FPGA: 5CSXFC6D6F31C6
    - 110K logic elements
    - 41,509 ALM blocks
    - 9 x 3.125 Gbps transceiver
    - 112 DSP blocks
    - Memory (Kb): 5,570 M10K; 621 MLAB

Xilinx Zynq

- 28 nm technology
- Processor System (PS)
  - 32 bit dual-core ARM® Cortex™-A9 MPCore
  - ARM AMBA AXI3 Interconnect
  - I/O peripherals
  - Memory interfaces
- Programmable Logic (PL)
  - Dynamical & partial reconfiguration
  - Complex logic block
  - 36 Kb Block RAM
  - 48 bit DSP



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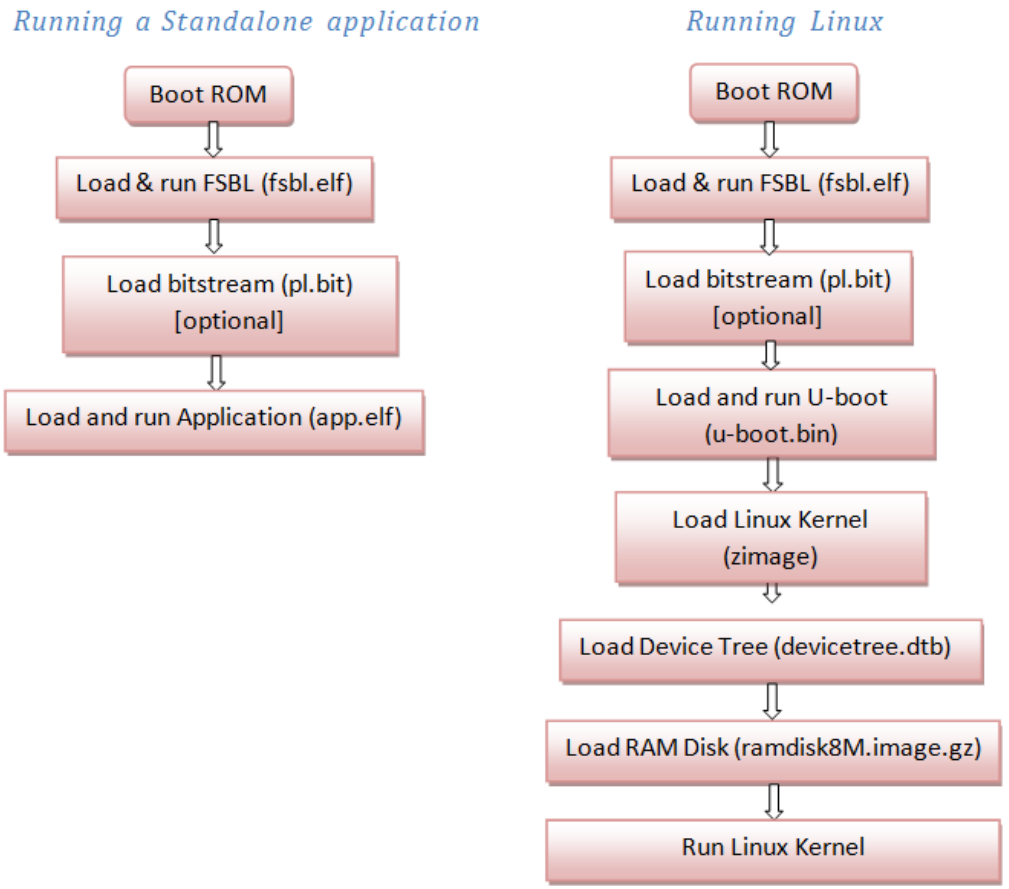
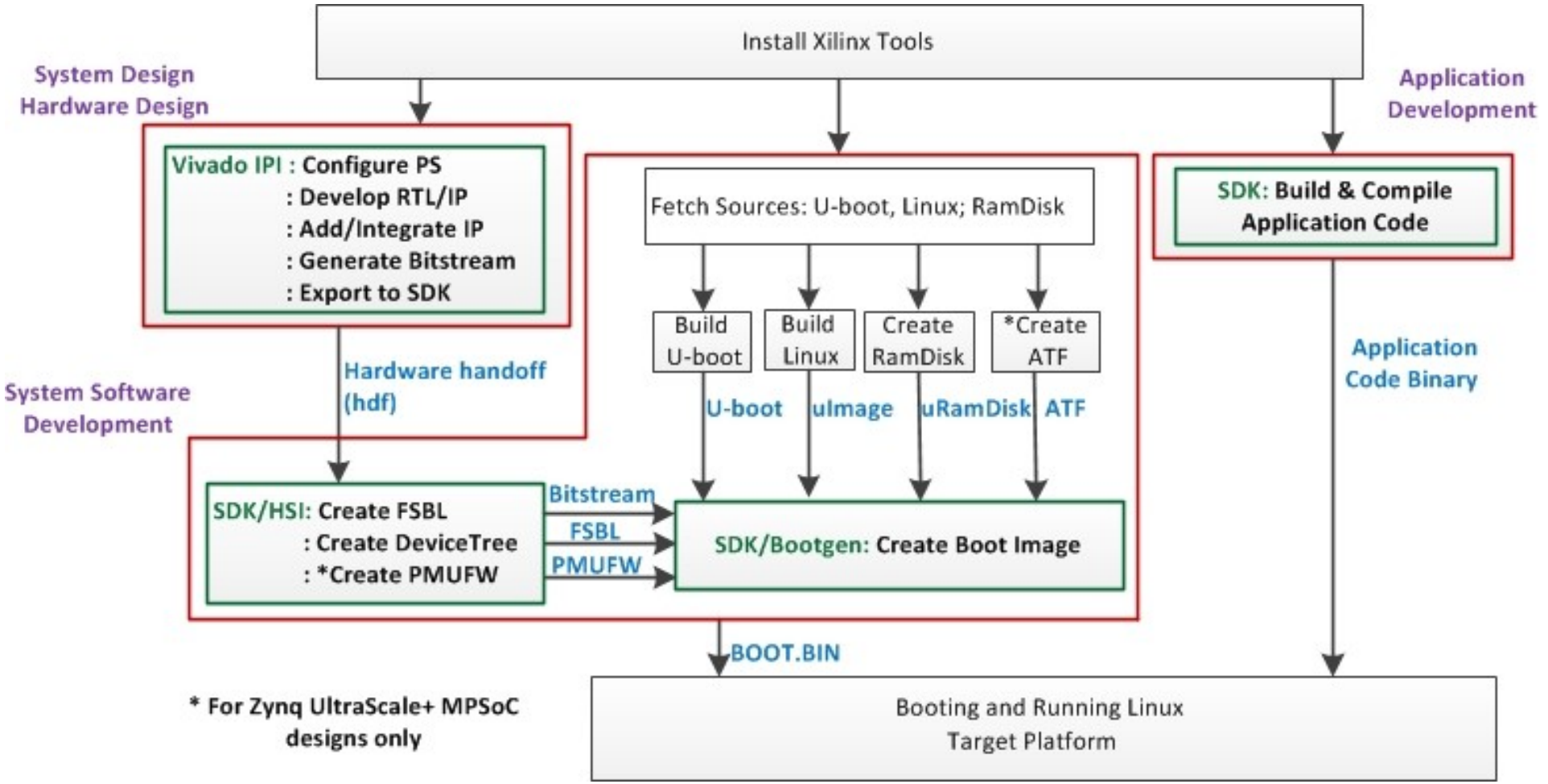
Xilinx Zynq Boot Flow



Xilinx Zynq Design Flow



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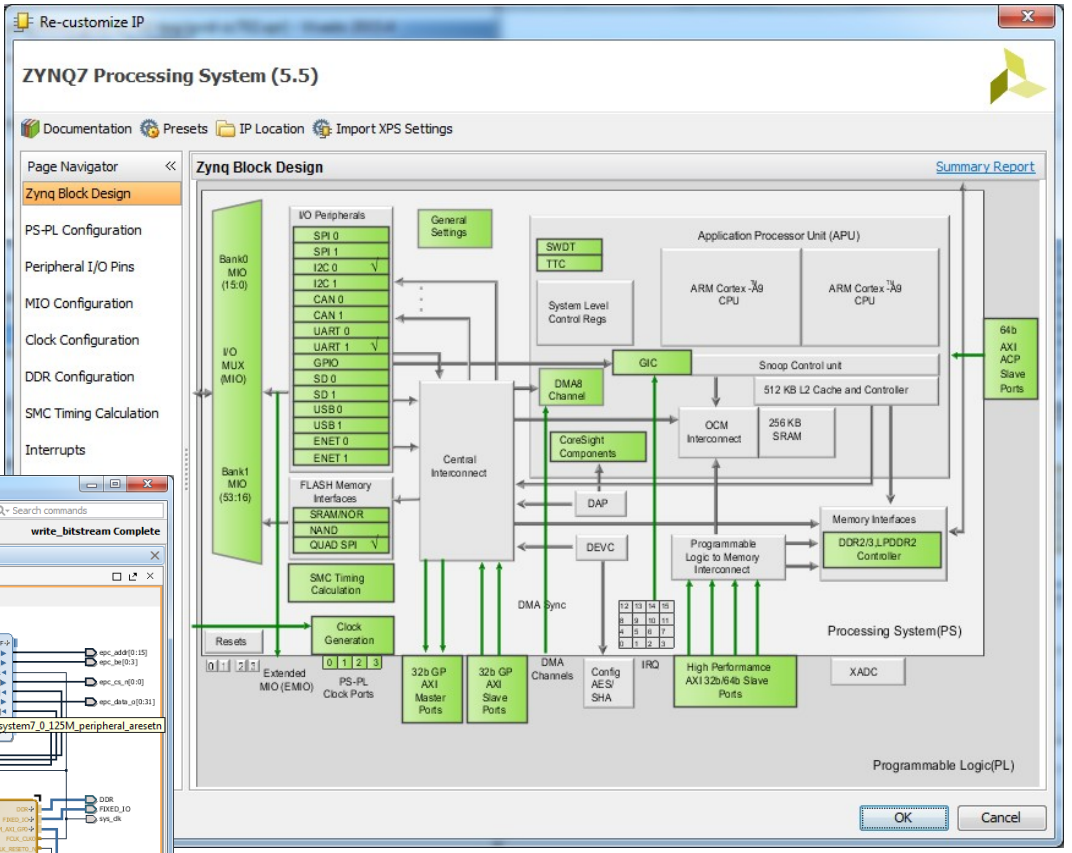
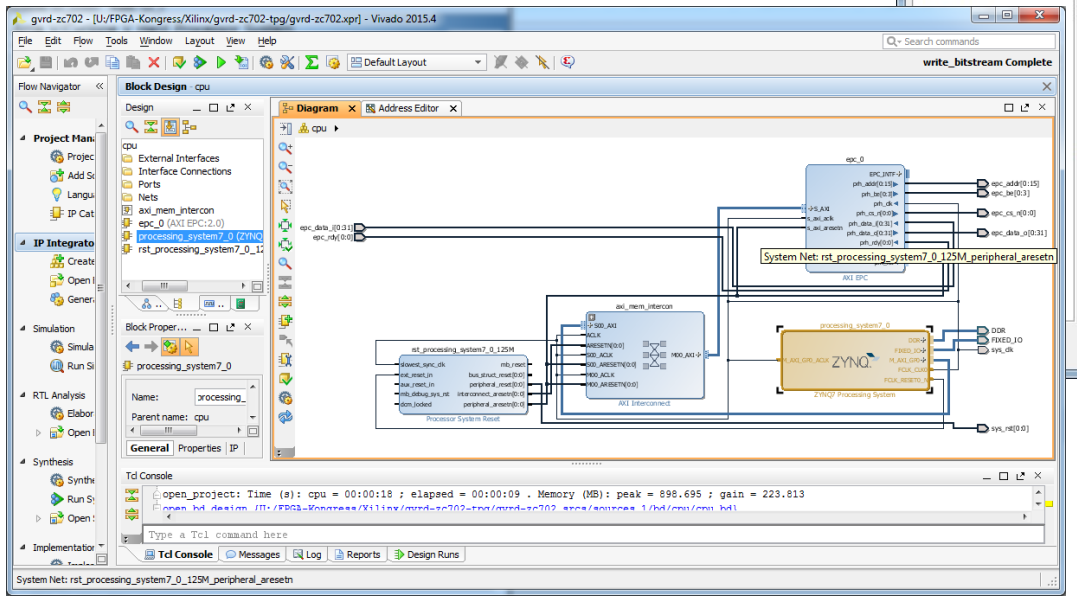
Zynq System Generation

- HW-Tools:
  - Vivado
  - Vivado IP Integrator





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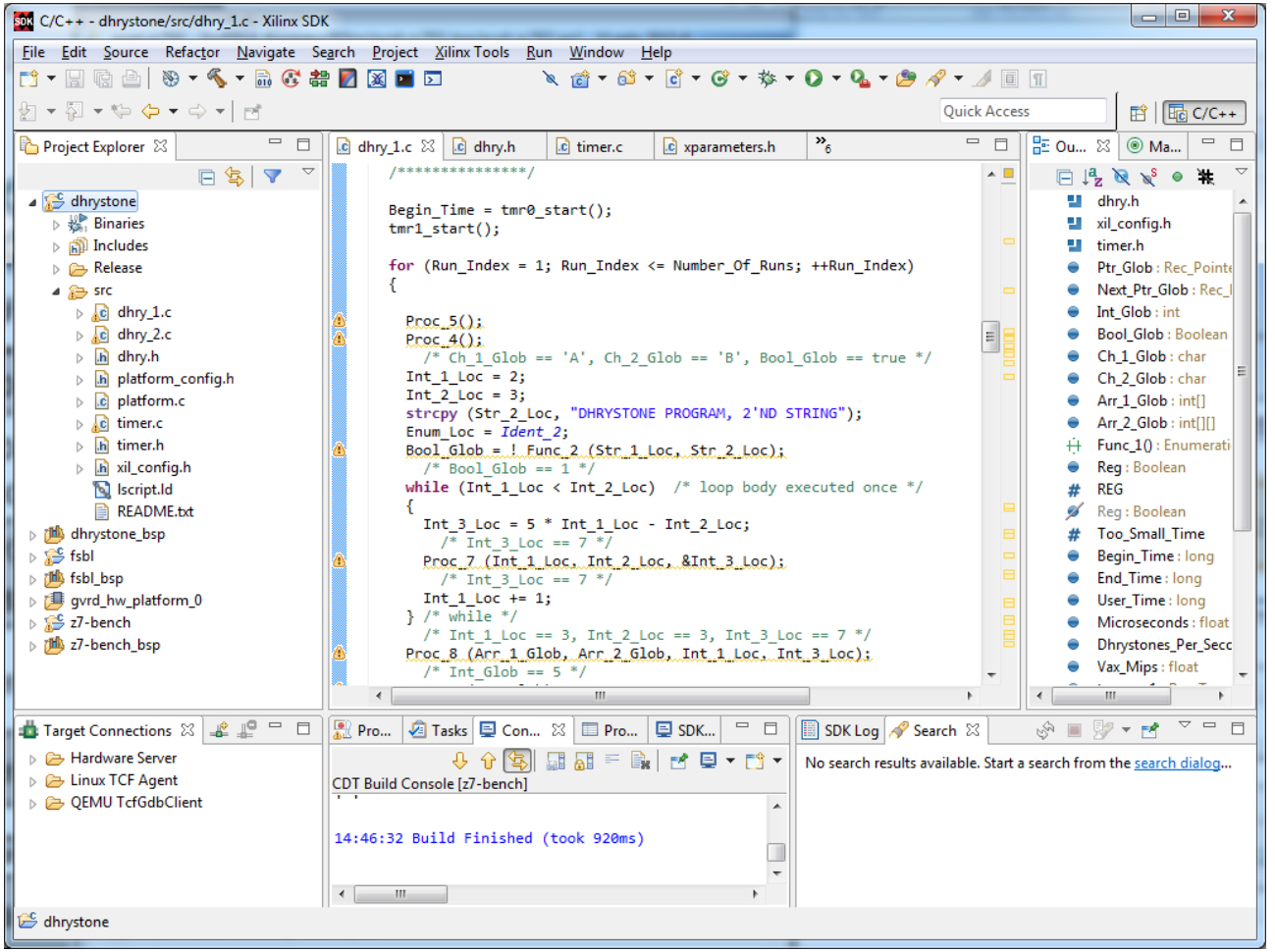
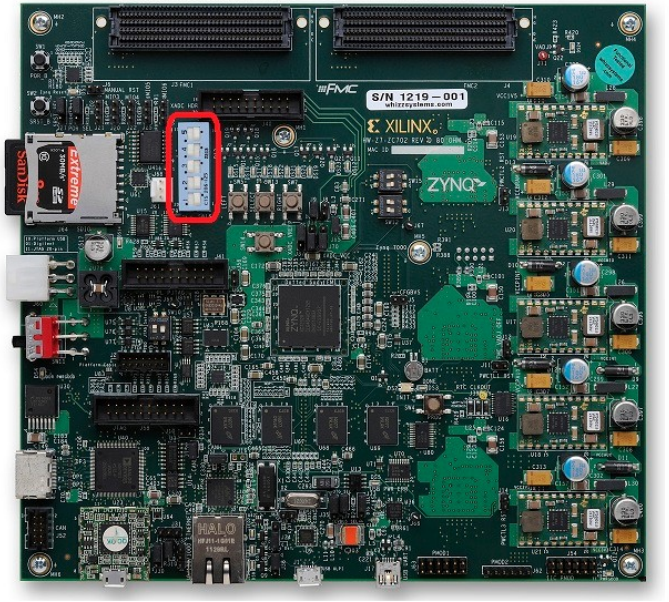
Zynq SW Development

- Xilinx SDK
- HW Platform
- FSBL
- Application



Xilinx Zynq Platform

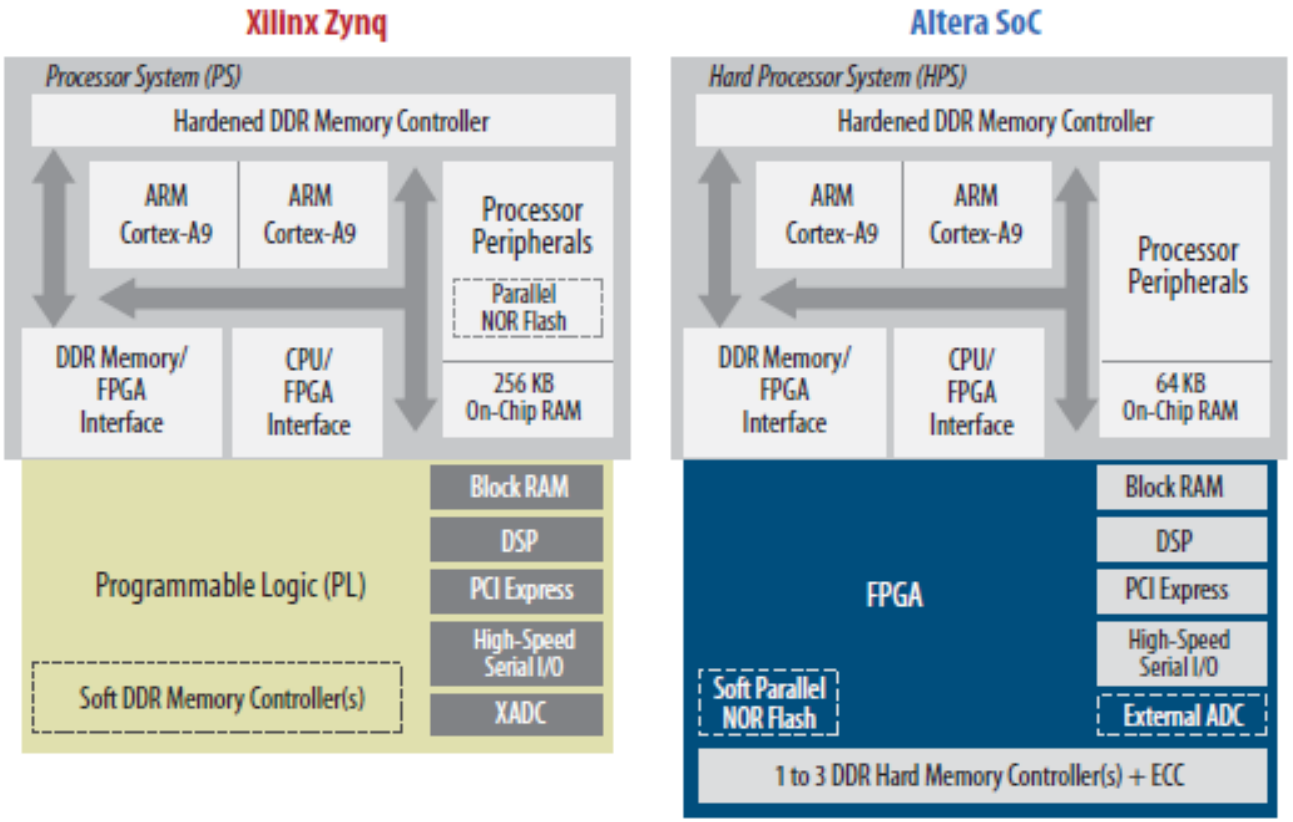
- Xilinx ZC702
  - FPGA: Zynq-7000 XC7Z020-1CLG484C AP SoC
    - 85K logic cells
    - 53,200 LUTs
    - 220 DSP slices
    - Block RAM (Mb): 4.9



Cyclone V Soc / Xilinx Zynq

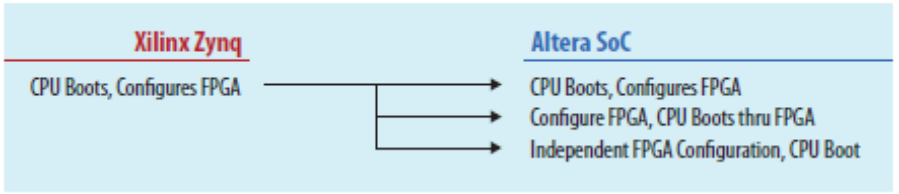
- High level comparison

Figure 1. High-Level Comparison of Zynq and Altera SoC Architectures



- Boot modes

Figure 3. Zynq and Altera SoC Boot and Configuration Modes



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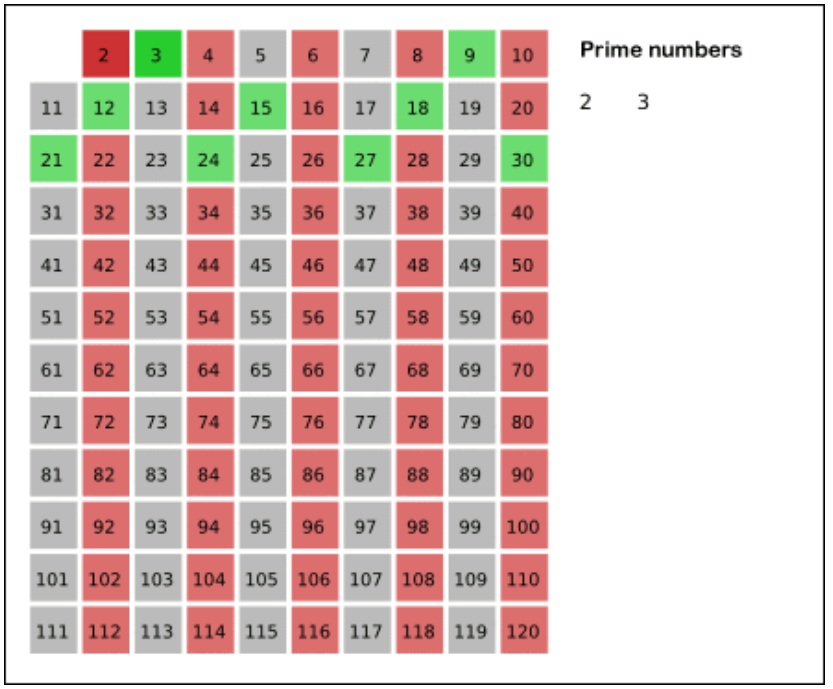
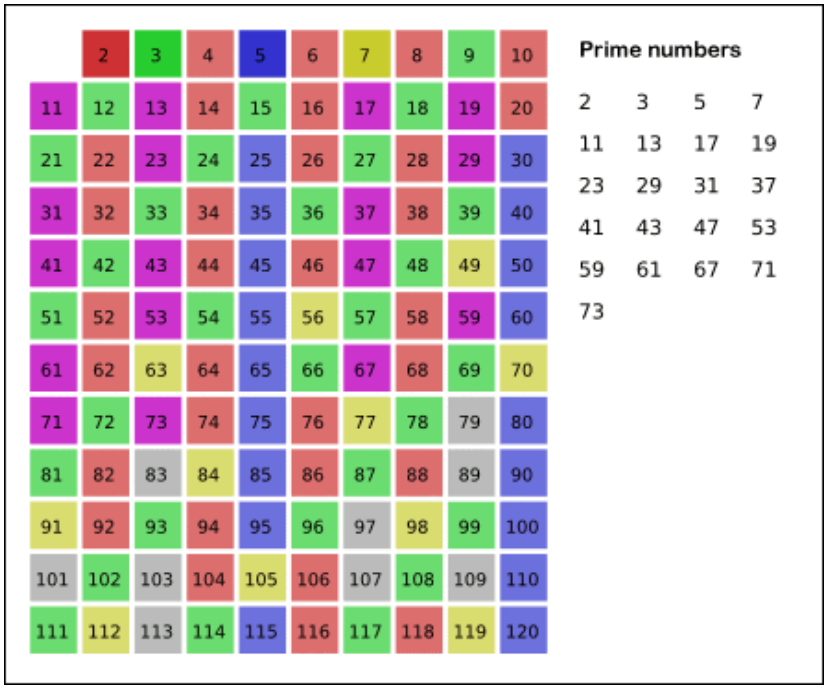
Benchmarks

- Sieve of Eratosthenes
- Dhrystone

Sieve of Eratosthenes

- Simple algorithm finding prime numbers up to a given integer
- List of all number from 2, 3, 4, … to max value N
- Iterative marking as “not prime” of multiples of each prime





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Sieve benchmark results 1/2

CPU	frequency [MHz]	N	duration	time unit
PB8051	48	2,000	608.00	ms
Nios II gen2	100	2,000	692.00	us
MicroBlaze	100	2,000	309.00	us
Cyclone V SoC BM	925	2,000	158.00	us
Zynq BM	666	2,000	6.40	us

CPU	frequency [MHz]	N	duration	time unit
Nios II gen2	100	15,000	5.79	ms
MicroBlaze	100	15,000	1.87	ms
Cyclone V SoC BM	925	15,000	1.20	ms
Zynq BM	666	15,000	26.26	us

Sieve benchmark results 2/2

CPU	frequency[MHz]	N	duration	time unit
Nios II gen2	100	20,000	Out of memory	
MicroBlaze	100	20,000	2.47	ms
Cyclone V SoC BM	925	200,000	16.89	ms
Cyclone V SoC Linux	925	200,000	6.00	ms
Zynq BM	666	200,000	0.33	ms
Zynq Linux	666	200,000	8.00	ms

CPU	frequency[MHz]	N	duration	time unit
Cyclone V Soc BM	925	2,000,000	177.59	ms
Cyclone V Soc Linux	925	2,000,000	68.00	ms
Zynq BM	666	2,000,000	3.70	ms
Zynq Linux	666	2,000,000	95.00	ms

Dhrystone 2.1

- 1984 by Reinhold Weicker, Siemens AG
  - First revision in Ada and Pascal
  - Now C version mainly used
- Synthetic performance benchmark
  - Easy-to-use
  - General-purpose (“integer”)
  - 12 different subroutines:
    - Pointer and array access operations
    - Simple arithmetic and logic operations
    - If statements and string operations
- Result: DMIPS(/MHz)
  - **D**hrystone **M**illion **I**nstructions **P**er **S**econd
  - 1 DMIPS = 1757 Dhrystones / s

Dhrystone benchmark results

CPU	frequency [MHz]	Dhrystone run [us]	Dhrystones / second	DMIPS / second	DMIPS / MHz
Nios II gen2	100	10.660	93,808	53.4	0.533
MicroBlaze	100	9.430	106,044	60.4	0.603
Zynq BM	666	0.324	3,086,419	1,756.6	2.637
Cyclone V SoC BM	925	8.320	120,180	68.4	0.073
Zynq Linux	666	0,482	2,075,980	1181,5	1,774
Cyclone V SoC Linux	925	0.347	2,884,616	1,641.8	1.775
Intel Core i3-4130	3,400	0.035	28,193,634	16,046.5	4.585

Thanks for your interest and time!

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