



# Comparison of CPU's in FPGA's

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# Agenda

- Overview
- CPU's
  - PB8051
  - Altera Nios II Gen2
  - Xilinx MicroBlaze
  - Altera Cyclone V SoC
  - Xilinx Zynq
- Benchmarks
  - Sieve of Eratosthenes
  - Dhrystone

# Sensor to Image GmbH

- Company

- Founded 1989 and privately owned
- Team of 9 developers, 2 people in production and 3 in administration
- Company goal: development, production and service of OEM image processing hardware tool
- Full service from training → development → layout → software → sample production → redesign → series production → support → repair is possible
- Production of 1000-2000 boards/year

- Development

- High speed and impedance controlled layout, pitch > 0.8 mm
- FPGA design tools experience with Altera, Xilinx, Lattice and MicroSemi tools
- FPGA simulation and verification with ModelSim 10.x
- Embedded C-Compilers for FPGA based 8051, Coldfire, MicroBlaze/NIOS, ARM in Zynq/Cyclone V SoC and BLACKFIN running Linux
- Capability for writing PC drivers VC6 – VC2015

- Production

- Semiautomatic Pick & Place machine with manual BGA placement and part handling down to size 0402
- Vapor phase oven for RoHS conform soldering PCB size ≤ 30x30 cm
- Thermal box for testing systems up to 50x50x50 cm under operation from -40° C up to 90° C
- Mixed signal oscilloscopes with bandwidth of 5 GHz

# Certificated & Applications

- EN ISO9001:2008 and EN ISO 14001:2009 certified procedures since 1996
- CE Production to EN 61000-6-3:2007 and EN 61000-6-4:2007 standard
- Production to MIL-STD-810E 501.3, ...502.3, ... 514.4-All, ... 516.4 and VG95328, VG95373 and VG96903
- Production to Marine standard EN 60945:2002
- Asia OEM application: inspection of copper in PCB production,  $\geq 700$  PCIe line scanning systems
- German OEM application: A0 printer & scanner electronics,  $\geq 2000$  CIS & USB3 IF boards
- American OEM application: 3D OEM camera, standard CMOS Sensor FPGA pre-processing and embedded Linux,  $\geq 1000$  system
- ...
- And you are welcome to verify this by yourself by visiting us in Schongau



# Typical S2I FPGA system

- Machine Vision FPGA IP vendor

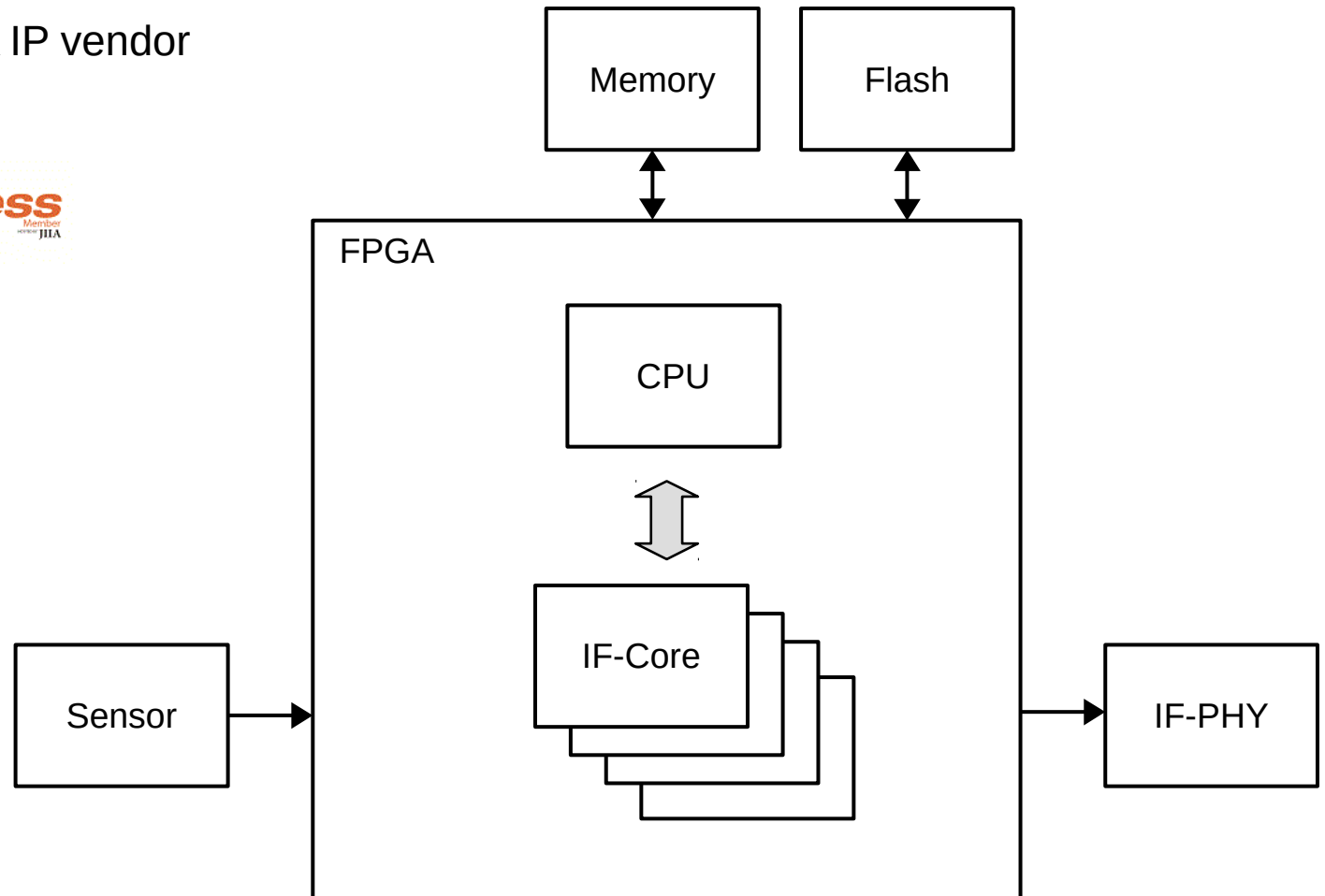


- FPGA's:

- Altera
- Xilinx
- Lattice
- MicroSemi

- CPU's:

- 8051
- Mico8/32
- Nios II
- MicroBlaze
- ARM A9 (C5 SoC / Zynq)

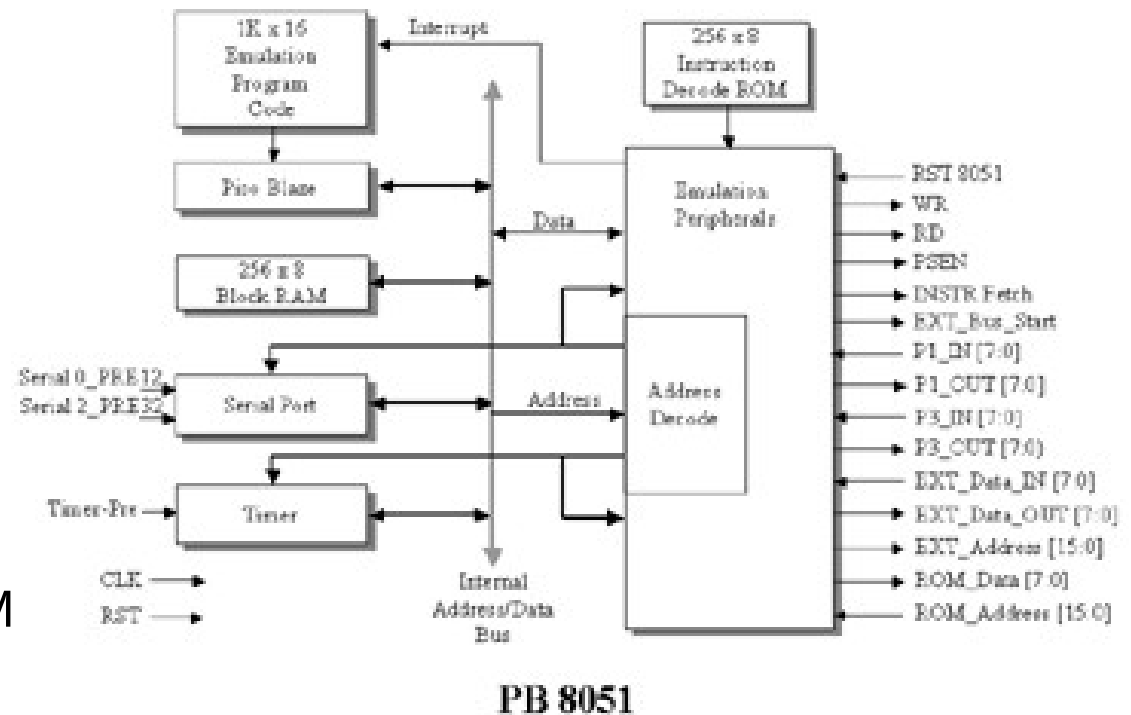


# CPU's

- PB8051
- Altera Nios II Gen2
- Xilinx MicroBlaze (9.5)
- Altera Cyclone V SoC
- Xilinx Zynq 7015

# PB8051

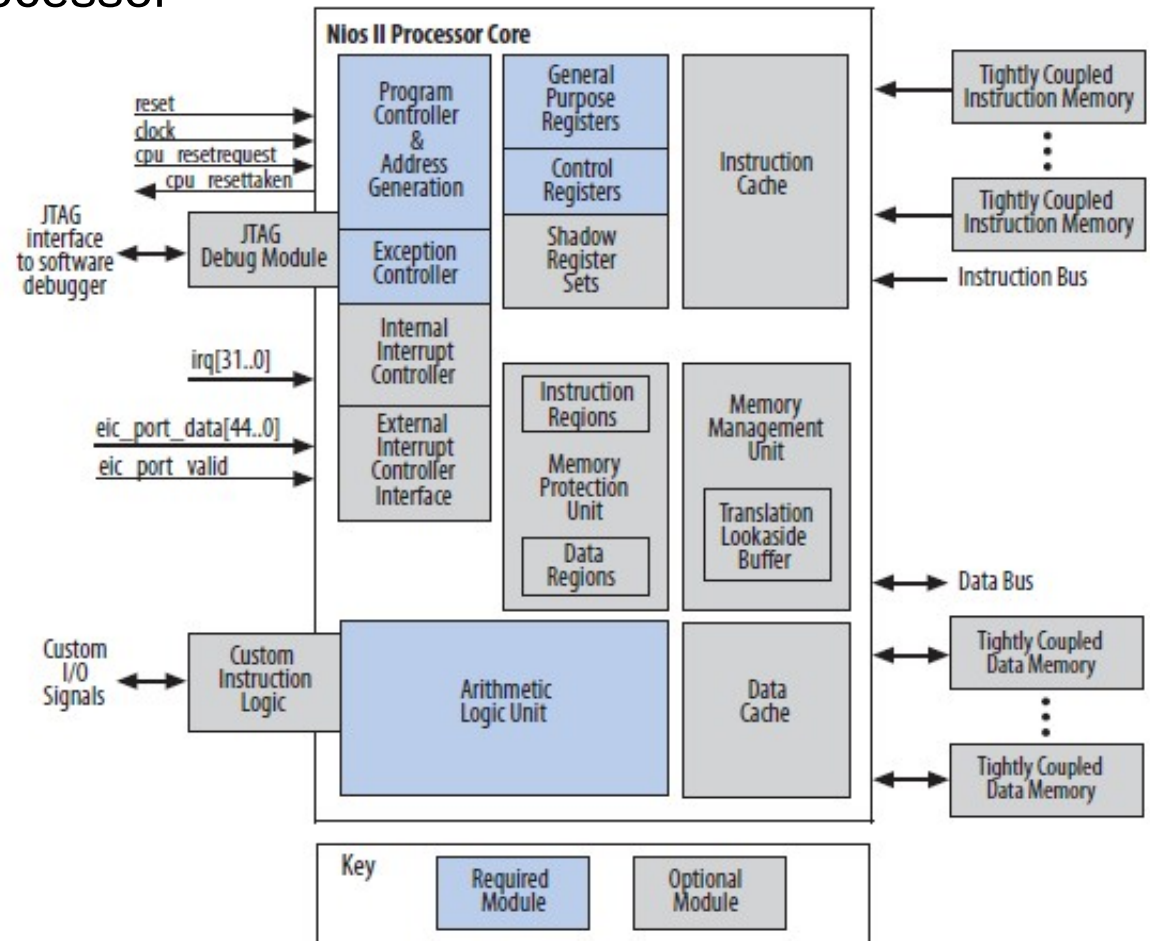
- 8-bit 8031 classic micro controller
- Build as a code interpreter to existing XILINX PicoBlaze or KCPSM6
- Not 1:1 compatible in code execution timing
- 1:1 compatible to existing compiler, OS and 8051 tools
- Can be run in different speeds to simplify clocking
- Very small, 350 slices plus BRAM for code/data
- No longer in maintenance and not tested in VIVADO



# Altera Nios II gen2

Figure 2-1: Nios II Processor Core Block Diagram

- 32-bit RISC embedded soft processor
- Little Endianness
- Interconnect:
  - Altera Avalon
  - ARM AMBA AXI
- Highly configurable
  - Memory Management Unit
  - Memory Protection Unit
  - ...
- 2 Variants:
  - Nios II/f
  - Nios II/e





# Nios II – System Design

- Qsys system integration tool
- IP Catalog
- Automatic generation of interconnect logic
- Support of Avalon, ARM, AMBA AXI, AMBA APB, AMBA AHB
- Hierarchical design flow
- Automatic HDL generation

The screenshot displays the Qsys system integration tool interface. The main window shows the 'System Contents' tab for a system named 'cpu'. It lists various components and their connections. The 'Parameters' window is open, showing the configuration for the 'Nios II Processor' (altera\_nios2\_gen2).

**System Contents Table:**

Use	Connections	Name	Description	Export	Clock	Base	End	IRQ
<input checked="" type="checkbox"/>		sys_pll	Altera PLL	sys_pll_locked	clk_50m			
<input checked="" type="checkbox"/>		locked	Conduit					
<input checked="" type="checkbox"/>		nios	Nios II Processor		[clk]			
<input checked="" type="checkbox"/>		data_master	Avalon Memory Mapped Master	Double-click to				
<input checked="" type="checkbox"/>		instruction_master	Avalon Memory Mapped Master	Double-click to				
<input checked="" type="checkbox"/>		irq	Interrupt Receiver	Double-click to	[clk]			IRQ 0
<input checked="" type="checkbox"/>		debug_mem_slave	Avalon Memory Mapped Slave	Double-click to	[clk]	# 0x0005_0800	0x0005_0fff	IRQ 31
<input checked="" type="checkbox"/>		custom_instruction_m...	Custom Instruction Master	Double-click to				
<input checked="" type="checkbox"/>		onchip_ram	On-Chip Memory (RAM or ROM)	Double-click to				
<input checked="" type="checkbox"/>		s1	Avalon Memory Mapped Slave	Double-click to	[clk-1]	0x0002_0000	0x0003_ffff	
<input checked="" type="checkbox"/>		jtag_uart	JTAG UART	Double-click to	[clk]			
<input checked="" type="checkbox"/>		avalon_jtag_slave	Avalon Memory Mapped Slave	Double-click to	[clk]	0x0005_1040	0x0005_1047	
<input checked="" type="checkbox"/>		irq	Interrupt Sender	Double-click to	[clk]			
<input checked="" type="checkbox"/>		rs232_uart	UART (RS-232 Serial Port)	Double-click to	[clk]			
<input checked="" type="checkbox"/>		s1	Avalon Memory Mapped Slave	Double-click to	[clk]	0x0005_1020	0x0005_103f	
<input checked="" type="checkbox"/>		external_connection	Conduit	Double-click to				
<input checked="" type="checkbox"/>		timer_0	Interval Timer	Double-click to	[clk]			
<input checked="" type="checkbox"/>		s1	Avalon Memory Mapped Slave	Double-click to	[clk]	0x0005_1000	0x0005_101f	
<input checked="" type="checkbox"/>		irq	Interrupt Sender	Double-click to	[clk]			
<input checked="" type="checkbox"/>		epc_tmr	Avalon MM Slave EPC Bridge IRQ	Double-click to	[clock]			
<input checked="" type="checkbox"/>		s0	Avalon Memory Mapped Slave	Double-click to	[clock]	0x0004_0000	0x0004_ffff	
<input checked="" type="checkbox"/>		epc	Conduit	Double-click to				
<input checked="" type="checkbox"/>		irq	Interrupt Sender	Double-click to	[clock]			

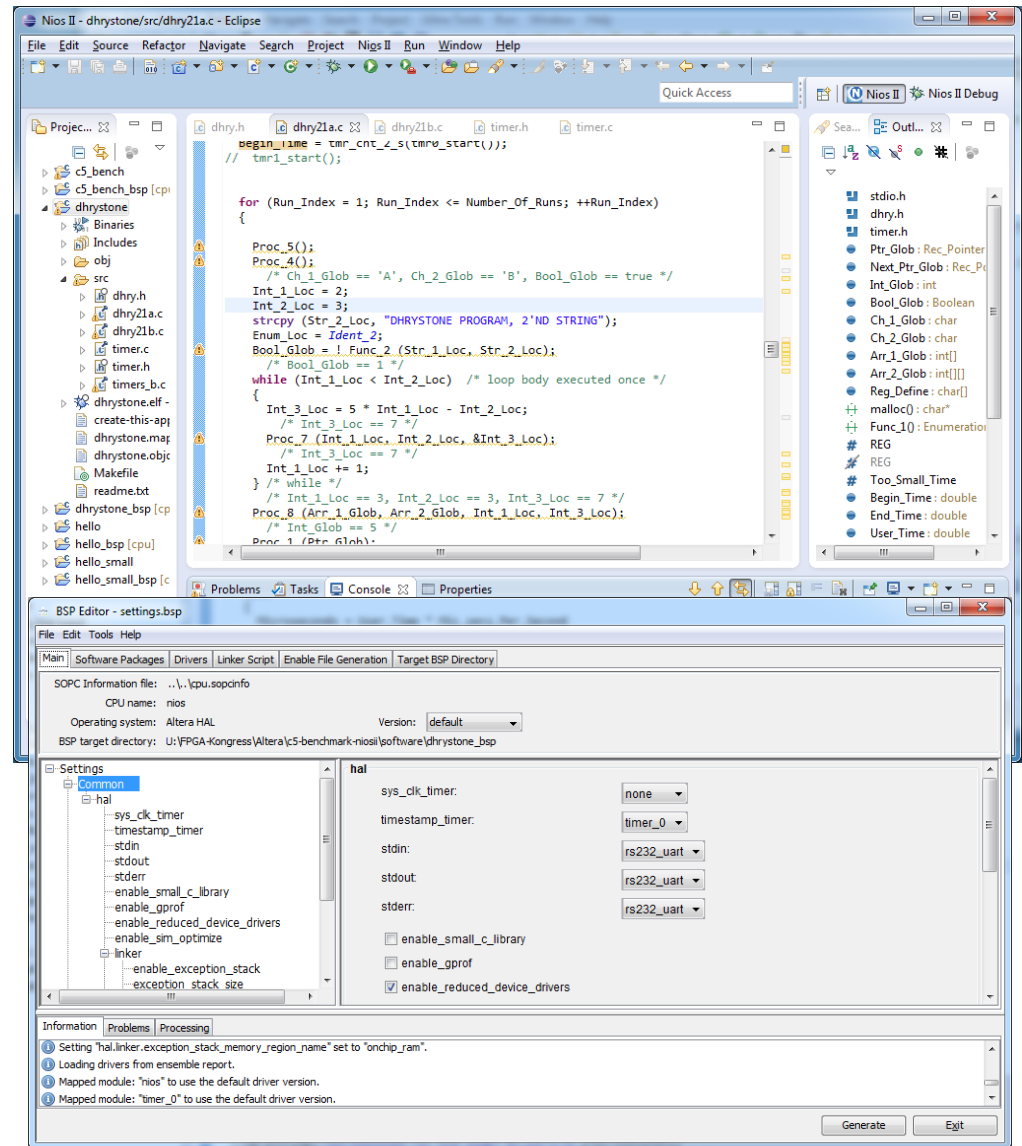
**Parameters Window: Nios II Processor (altera\_nios2\_gen2)**

Select an Implementation:  Nios II/e  Nios II/f

	Nios II/e	Nios II/f
<b>Summary</b>	Resource-optimized 32-bit RISC	Performance-optimized 32-bit RISC
<b>Features</b>	JTAG Debug	JTAG Debug Hardware Multiply/Divide Instruction/Data Caches Tightly-Coupled Masters ECC RAM Protection External Interrupt Controller Shadow Register Sets MPU MMU
<b>RAM Usage</b>	2 + Options	2 + Options

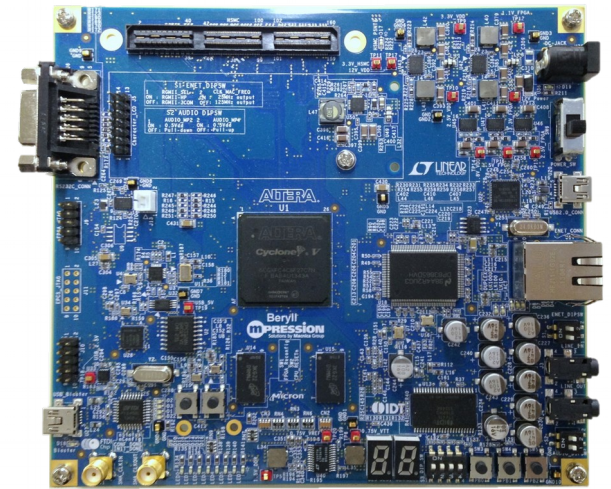
# Nios II – SW Development

- Nios II Embedded Design Suite
  - Nios II Software Build Tools for Eclipse
  - Compilers
  - Debuggers
  - Device drivers
  - Bare metal HAL
  - Nios II Command Shell
  - System Console
- `<design>.sopcinfo`
  - BSP generation
- `system.h`



# Nios II – HW Platform

- MPRESSION Beryll – Cyclone V GX Baseboard
  - FPGA: 5CGXFC4C6F27C7N
    - 50K logic elements
    - 18,868 ALM blocks
    - 6 x 3.125 Gbps transceiver
    - 70 DSP blocks
    - Memory (Kb): 2,500 M10K; 295 MLAB
- Benchmark Design
  - Logic utilization (in ALMs): 1,476 / 18,860 (8%)
  - Total RAM blocks: 128 / 250
- Nios II of Benchmark Design
  - Logic utilization (in ALMs): 842
  - Total RAM blocks: 8
  - f\_max: 128 MHz



# Xilinx MicroBlaze

- 32-bit RISC embedded soft processor
- Big/Little Endianness
- Interconnect:
  - PLB / LMB
  - AXI
- Highly configurable
  - Memory Management Unit
  - Floating-Point Unit
  - ...
- 6 Variants

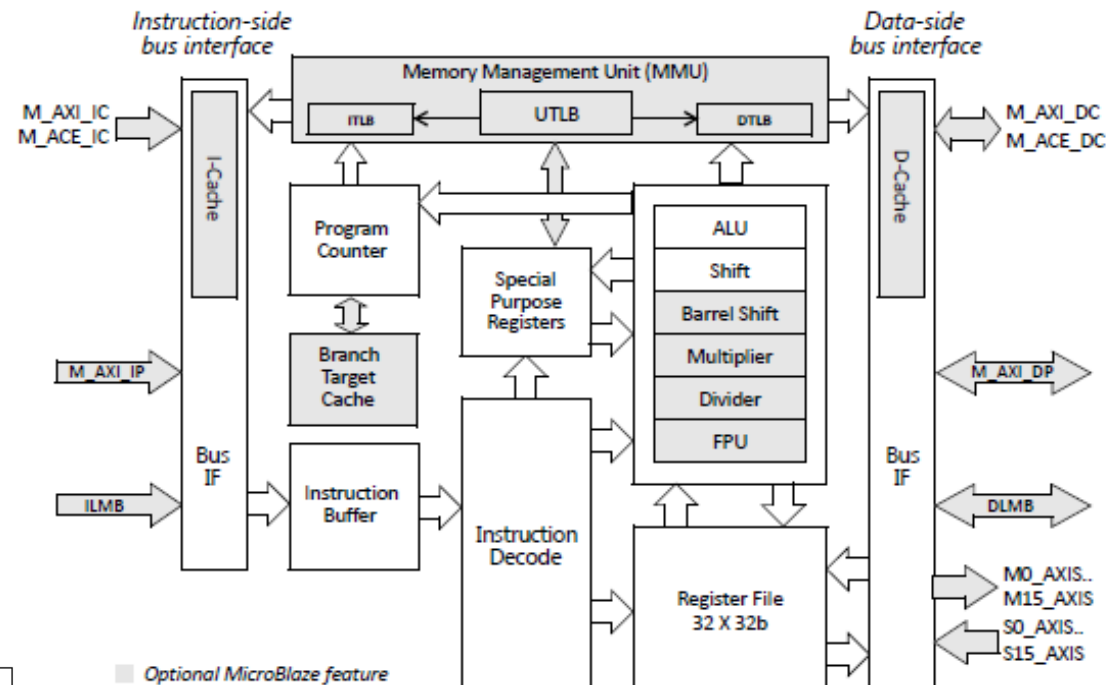


Figure 2-1: MicroBlaze Core Block Diagram

Table A-4: Device Utilization - Artix-7 FPGAs (XC7A200T fbg676-3)

Configuration	Device Resources		
	LUTs	FFs	F <sub>max</sub> (MHz)
Minimum Area	648	214	234
Maximum Performance	3879	3064	154
Maximum Frequency	906	545	234
Linux with MMU	3653	3218	142
Low-end Linux with MMU	3108	2582	153
Typical	2070	1777	190

# MicroBlaze – System Design

- Vivado IP Integrator
- IP Catalog
- Supports intelligent auto-connection

The image displays the Vivado 2015.4 software interface for system design. The main window shows a block design for a CPU, featuring a central MicroBlaze processor connected to various peripherals including local memory, peripheral modules, and an AXI interconnect. The interface includes a Project Manager on the left, an Address Editor, and a Diagram view.

Two configuration windows for the MicroBlaze (9.5) IP are overlaid. The top-left window shows the 'Resources' tab with a bar chart of Resource Estimates (Frequency, Area, Performance) and a 'General' tab with various configuration options. The bottom-right window shows the 'Welcome to MicroBlaze Configuration Wizard' dialog, which includes a 'Resources' tab and a 'General Settings' section with checkboxes for various features like 'Enable MicroBlaze Linux with MMU' and 'Use Instruction and Data Caches'.

**Resource Estimates (from top-left window):**

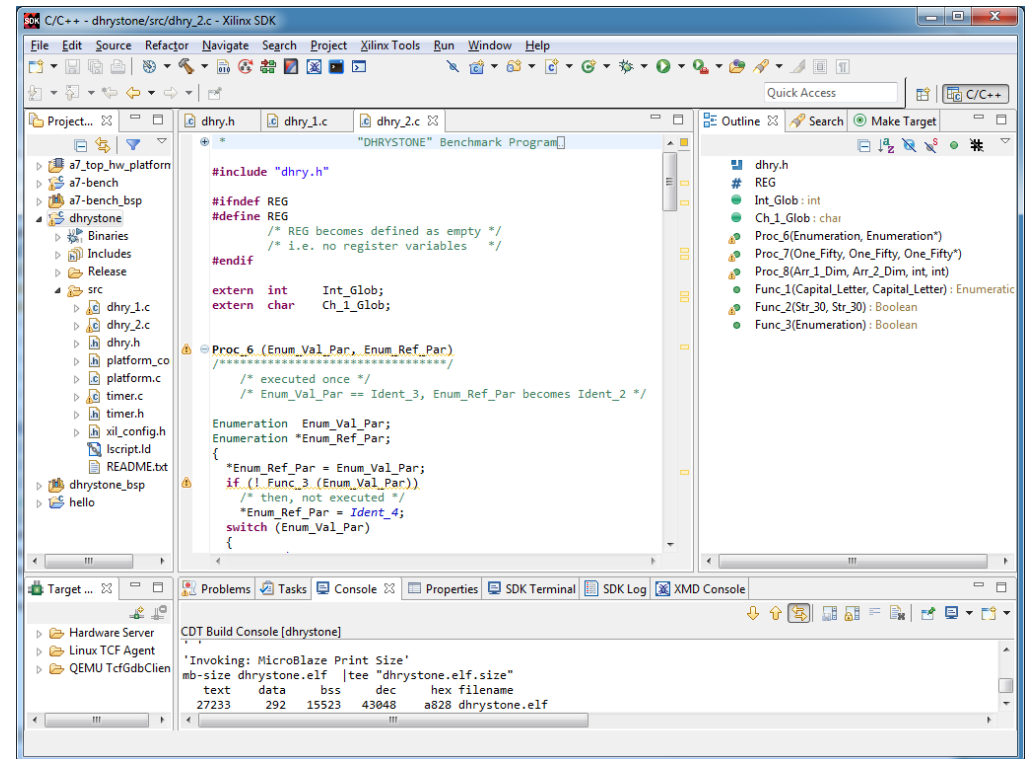
Resource	Frequency (%)	Area (%)	Performance (%)
BRAM	~100	~15	~10
DSP48E1	~15	~10	~10

**General Settings (from bottom-right window):**

- Select Implementation to optimize area (with lower instruction throughput)
- Enable Branch Target Cache
- Branch Target Cache Size: DEFAULT
- Fault Tolerance:  Auto  Enable Fault Tolerance Support

# MicroBlaze – SW Development

- XSDK (Xilinx Software Development Kit)
  - Compilers
  - Debugger
  - Device drivers
  - Libraries
  - XMD Console
- <design>.hdf
  - HW platform generation
- xparameters.h



The screenshot displays the Xilinx IDE interface. The main editor window shows the source code for `dhry_2.c`, which includes `dhry.h` and defines a benchmark program. The code includes a `Proc_6` function that performs a series of operations on enumeration and integer variables. The XMD Console at the bottom shows the output of the build process, including the command `'Invoking: MicroBlaze Print Size'` and the resulting size information for the `dhrystone.elf` file.

```
#include "dhry.h"

#ifdef REG
/* REG becomes defined as empty */
/* i.e. no register variables */
#endif

extern int Int_Glob;
extern char Ch_1_Glob;

Proc_6 (Enum_Val_Par, Enum_Ref_Par)
/******
/* executed once */
/* Enum_Val_Par == Ident_3, Enum_Ref_Par becomes Ident_2 */

Enumeration Enum_Val_Par;
Enumeration *Enum_Ref_Par;
{
  *Enum_Ref_Par = Enum_Val_Par;
  if (!Func_3 (Enum_Val_Par))
    /* then, not executed */
    *Enum_Ref_Par = Ident_4;
  switch (Enum_Val_Par)
  {
```

CDT Build Console [dhrystone]

```
'Invoking: MicroBlaze Print Size'
mb-size dhrystone.elf |tee "dhrystone.elf.size"
text data bss dec hex filename
27233 292 15523 43048 a828 dhrystone.elf
```

# MicroBlaze – Platform

- Xilinx AC701

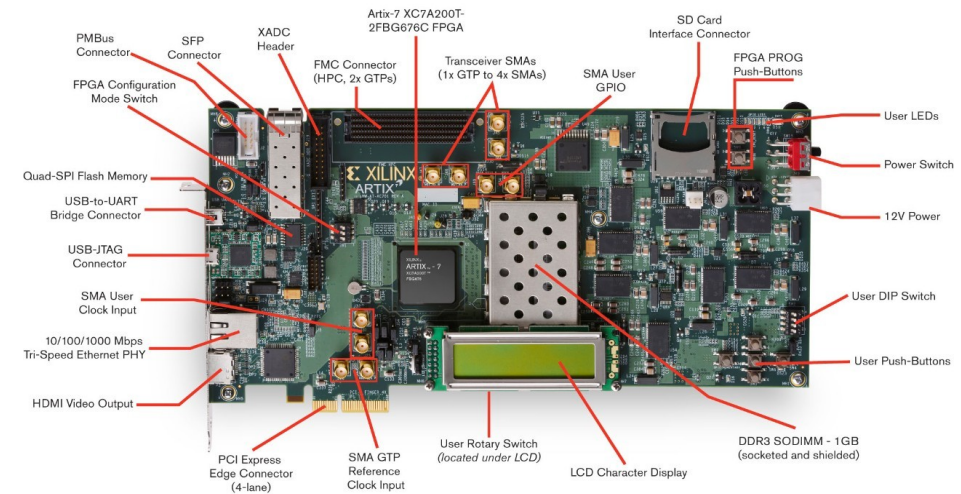
- FPGA: Artix-7 XC7A200T-2FBG676C
  - 215,360 logic cells
  - 269,200 FFs
  - 740 DSP slices
  - Block RAM (Kb): 12,140

- Benchmark Design

- Logic utilization:
  - LUTs: 1,888 / 134,600 (1.40%)
  - FFs: 1,736 / 269,200 (0.64%)
- BRAM: 32 / 365

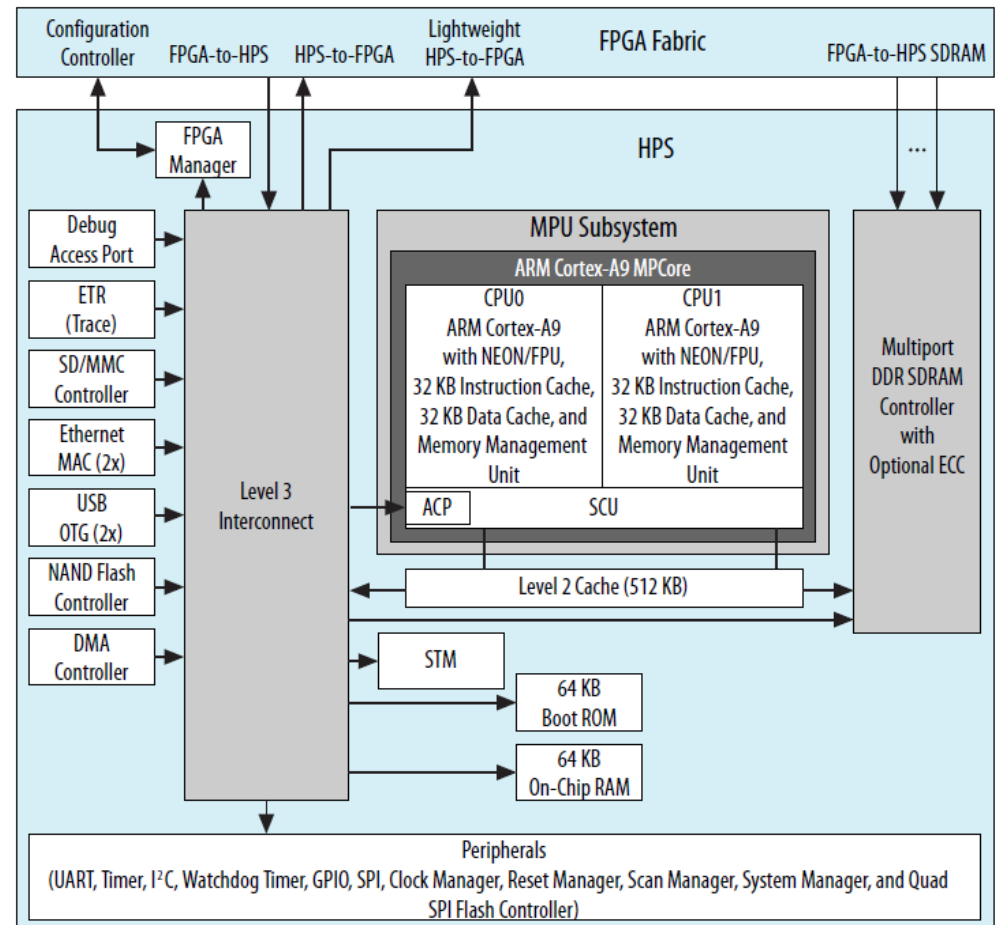
- Microblaze of Benchmark Design

- LUTs: 1118
- FFs: 926
- f\_max: 137 MHz



# Cyclone V SoC

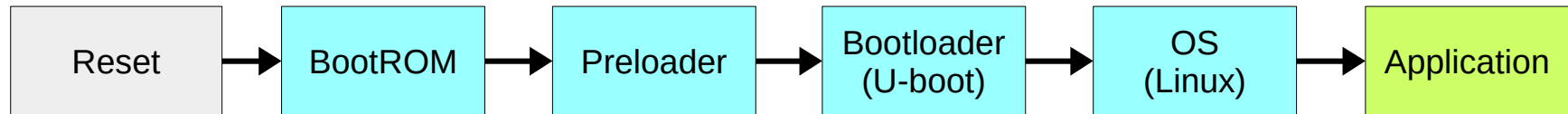
- 28 nm Low Power (28LP) process
- Hard Processor System (HPS)
  - 32 bit dual-core ARM® Cortex™-A9 MPCore
  - HPS-FPGA Bridge (Avalon, AXI3)
  - I/O peripherals
- FPGA Fabric
  - Dynamical & partial reconfiguration
  - Hard-IPs (DSP, PCIe, Memory Controller)
  - Complex logic block
  - 10 Kb Block RAM with ECC
- [rocketboards.org](http://rocketboards.org)
  - RefDesigns, tutorial, ...



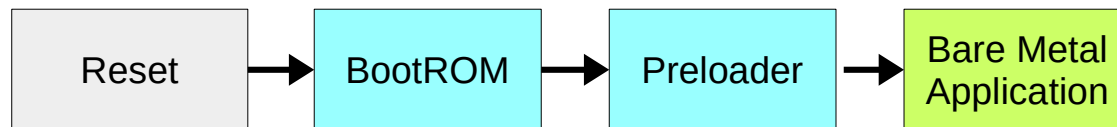


# Altera SoC Boot Flow

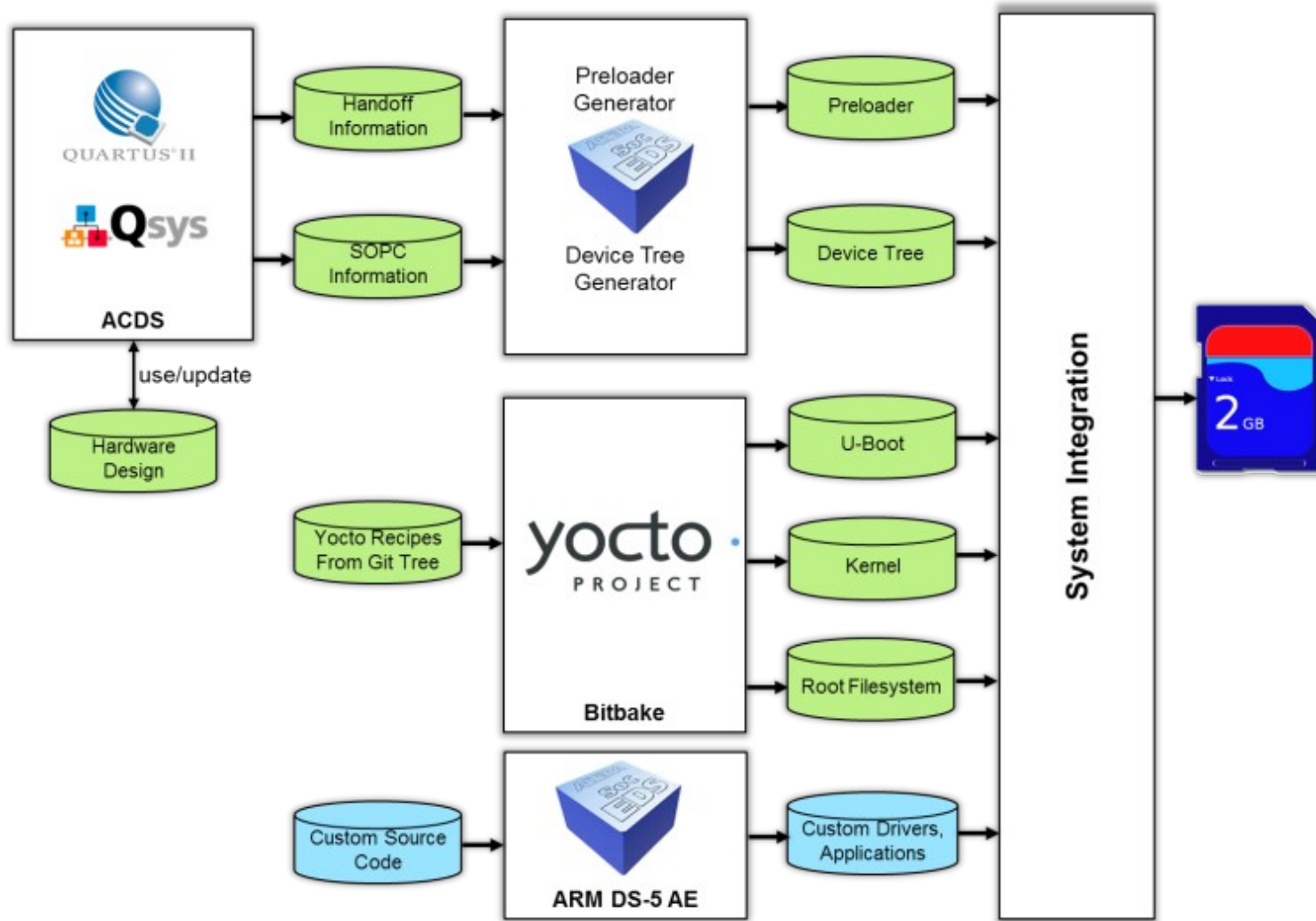
- Boot flow of typical operating system



- Boot flow of bare metal application

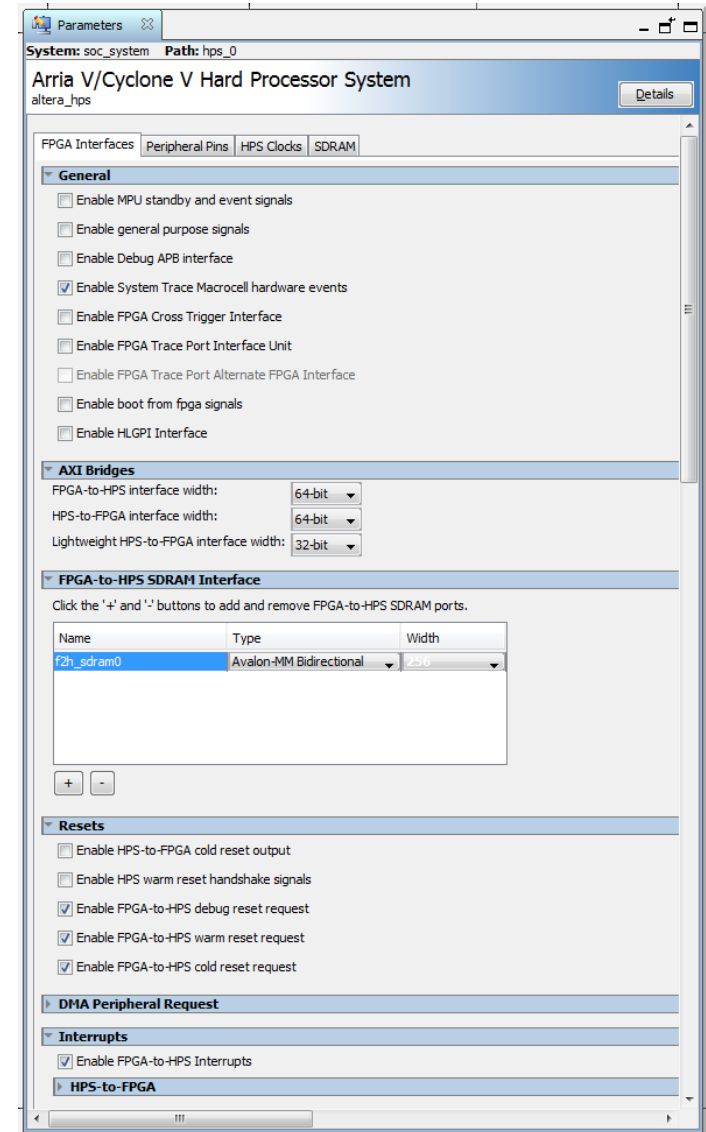
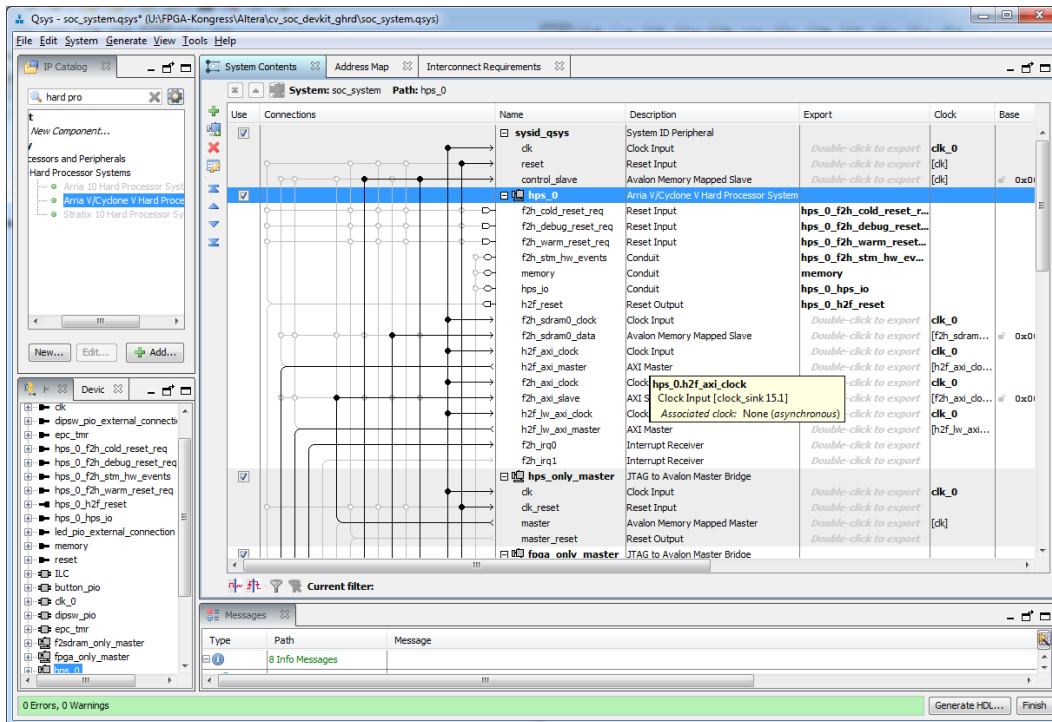


# Cyclone V SoC Design Flow



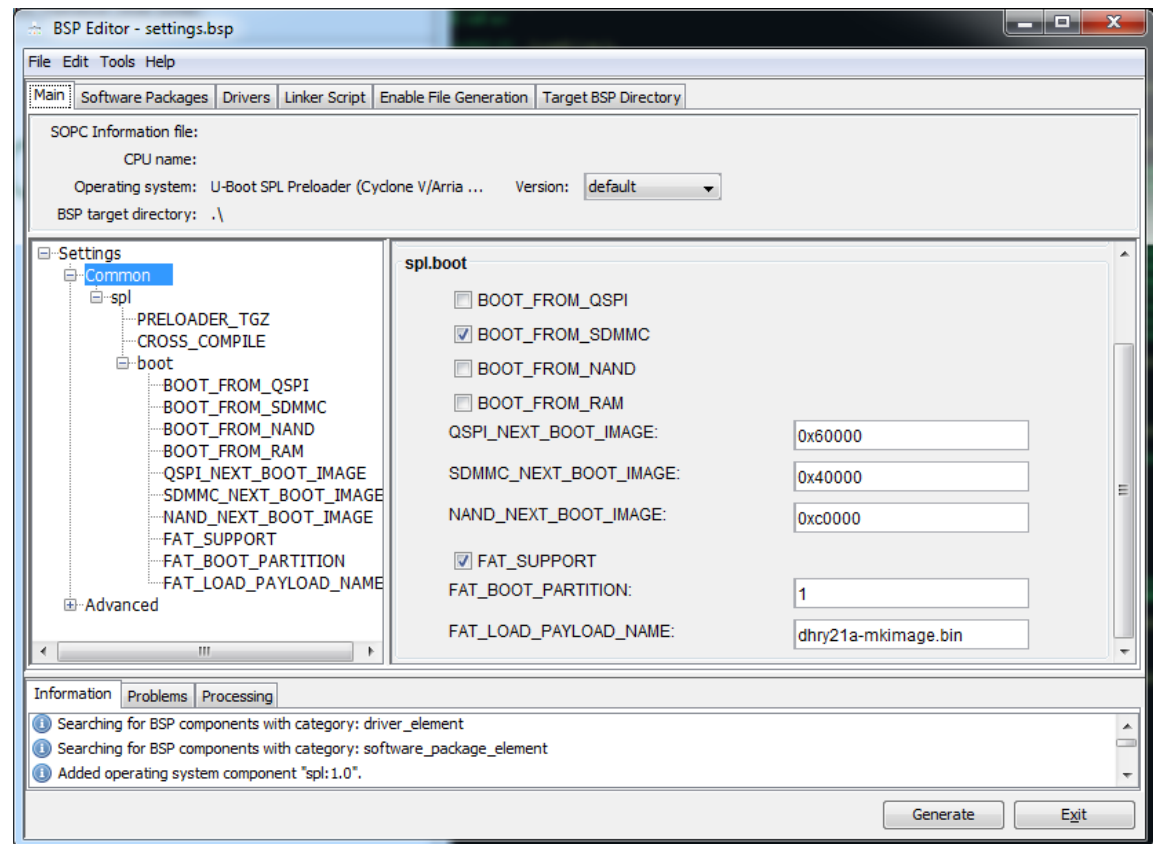
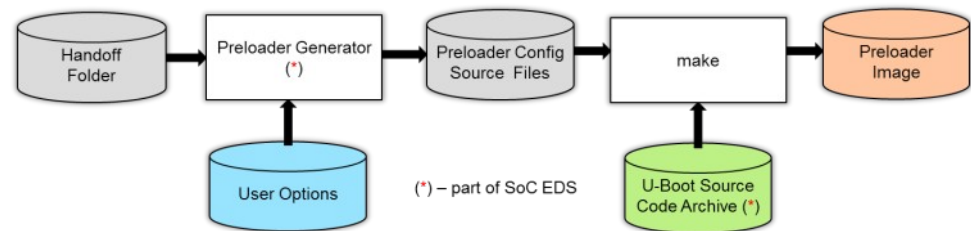
# Cyclone V SoC – System Design

- Tools: Quartus, Qsys



# Cyclone V SoC – Preloader

- Embedded Command Shell
- Preloader Generation
  - BSP-Editor



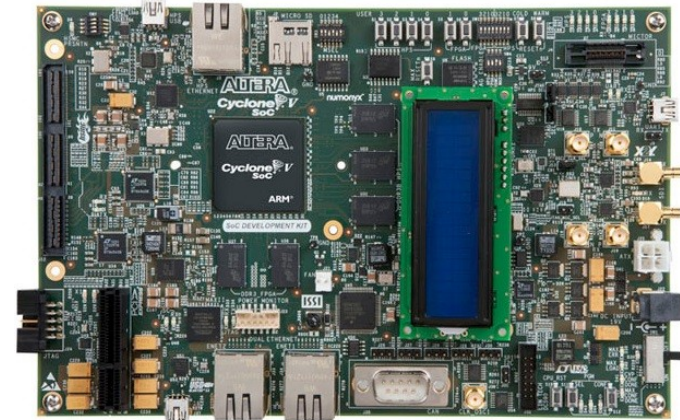
# Cyclone V SoC – SW Development

- ARM DS-5 Altera Edition
  - No system.h  
Generate Qsys headers instead
  - Extra license needed for debugging

```
C/C++ - Dhrystone/dhry21a.c - Eclipse Platform
File Edit Source Refactor Navigate Search Project Run Window Help
Quick Access
Project Explorer
cv_soc_bench
Dhrystone
  Includes
  Debug
  qsys_headers
  Release
  dhry.h
  dhry21a.c
  dhry21b.c
  timer.c
  timer.h
  tmp
  cycloneV-dk-ram-modifi
  dhry21a_c
  dhry21a-mkimage.bin
  dhry21a.axf
  dhry21a.bin
  dhry21a.o
  dhry21b.o
  Makefile
  timer.o
dhry21a.c
253 // printf ("tmr0_cnt = 0x%08X\r\n", tmr0_cnt);
254 Begin_Time = tmr_cnt_2_s(tmr0_start());
255
256
257 for (Run_Index = 1; Run_Index <= Number_Of_Runs; ++Run_Index)
258 {
259
260 Proc_5();
261 Proc_4();
262 /* Ch_1_Glob == 'A', Ch_2_Glob == 'B', Bool_Glob == true */
263 Int_1_Loc = 2;
264 Int_2_Loc = 3;
265 strcpy (Str_2_Loc, "DHRYSTONE PROGRAM, 2'ND STRING");
266 Enum_Loc = Ident_2;
267 Bool_Glob = ! Func_2 (Str_1_Loc, Str_2_Loc);
268 /* Bool_Glob == 1 */
269 while (Int_1_Loc < Int_2_Loc) /* loop body executed once */
270 {
271 Int_3_Loc = 5 * Int_1_Loc - Int_2_Loc;
272 /* Int_3_Loc == 7 */
273 Proc_7 (Int_1_Loc, Int_2_Loc, &Int_3_Loc);
274 /* Int_3_Loc == 7 */
275 Int_1_Loc += 1;
276 } /* while */
277 /* Int_1_Loc == 3, Int_2_Loc == 3, Int_3_Loc == 7 */
278 Proc_8 (Arr_1_Glob, Arr_2_Glob, Int_1_Loc, Int_3_Loc);
dhry.h
timer.h
Ptr_Glob : Rec_Pointer
Next_Ptr_Glob : Rec_Pointer
Int_Glob : int
Bool_Glob : Boolean
Ch_1_Glob : char
Ch_2_Glob : char
Arr_1_Glob : int[]
Arr_2_Glob : int[][]
Reg_Define : char[]
malloc() : char*
Func_10() : Enumeration
REG
REG
Too_Small_Time
Begin_Time : float
End_Time : float
User_Time : float
Microseconds : float
Problems Tasks Console Properties
CDT Build Console [Dhrystone]
i:/altera/15.1/embedded/host_tools/mentor/gnu/arm/baremetal/bin/./lib/gcc/arm-altera-eabi/4.9.2/../../../../a
i:/altera/15.1/embedded/host_tools/mentor/gnu/arm/baremetal/bin/./lib/gcc/arm-altera-eabi/4.9.2/../../../../a
i:/altera/15.1/embedded/host_tools/mentor/gnu/arm/baremetal/bin/./lib/gcc/arm-altera-eabi/4.9.2/../../../../a
'Finished building target: Dhrystone.axf'
```

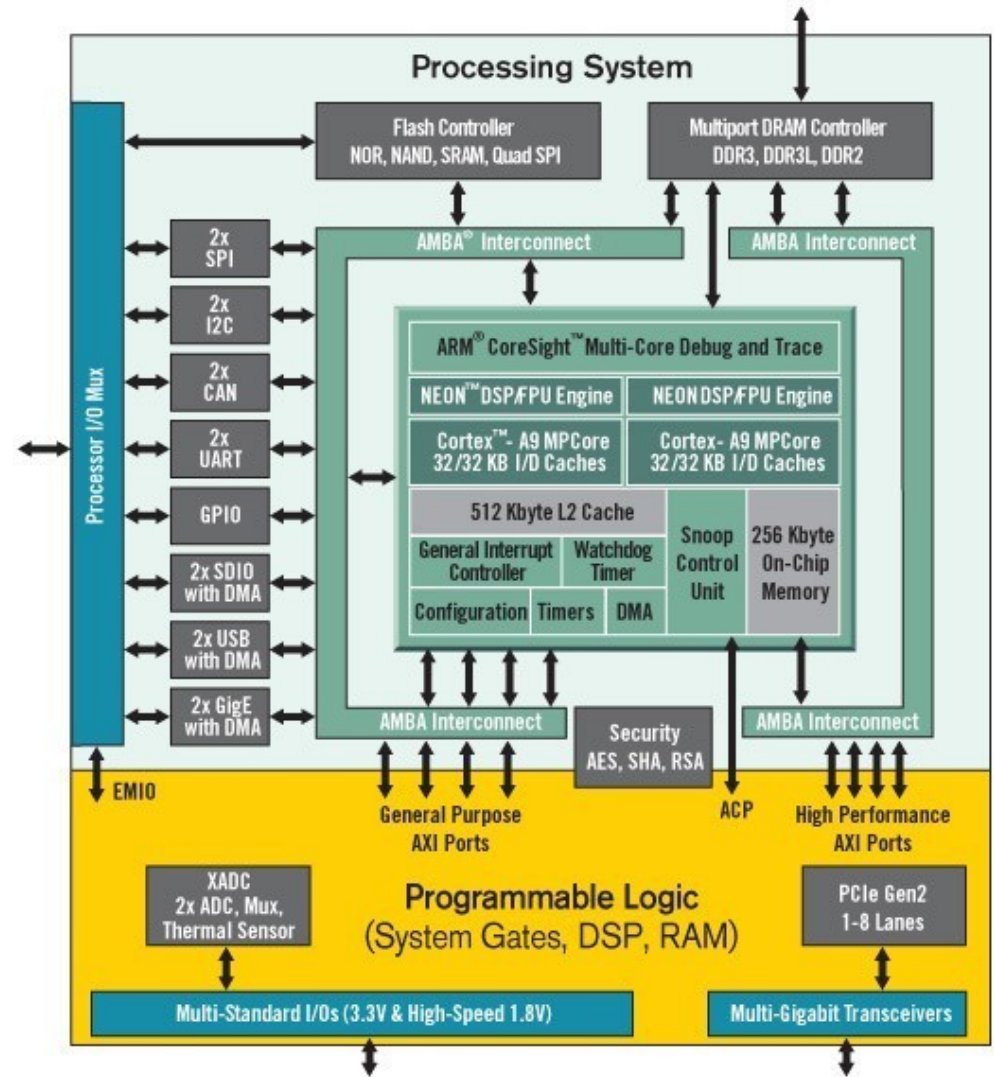
# Cyclone V SoC Platform

- Cyclone V SoC Development Board
  - FPGA: 5CSXFC6D6F31C6
    - 110K logic elements
    - 41,509 ALM blocks
    - 9 x 3.125 Gbps transceiver
    - 112 DSP blocks
    - Memory (Kb): 5,570 M10K; 621 MLAB



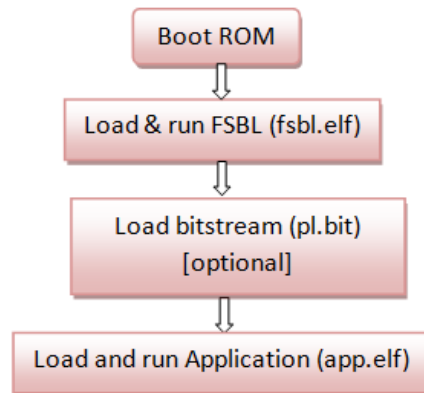
# Xilinx Zynq

- 28 nm technology
- Processor System (PS)
  - 32 bit dual-core ARM® Cortex™-A9 MPCore
  - ARM AMBA AXI3 Interconnect
  - I/O peripherals
  - Memory interfaces
- Programmable Logic (PL)
  - Dynamical & partial reconfiguration
  - Complex logic block
  - 36 Kb Block RAM
  - 48 bit DSP

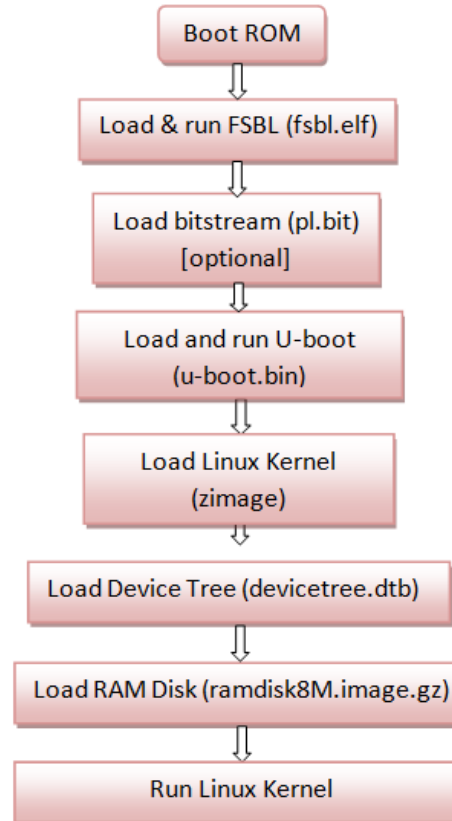


# Xilinx Zynq Boot Flow

*Running a Standalone application*

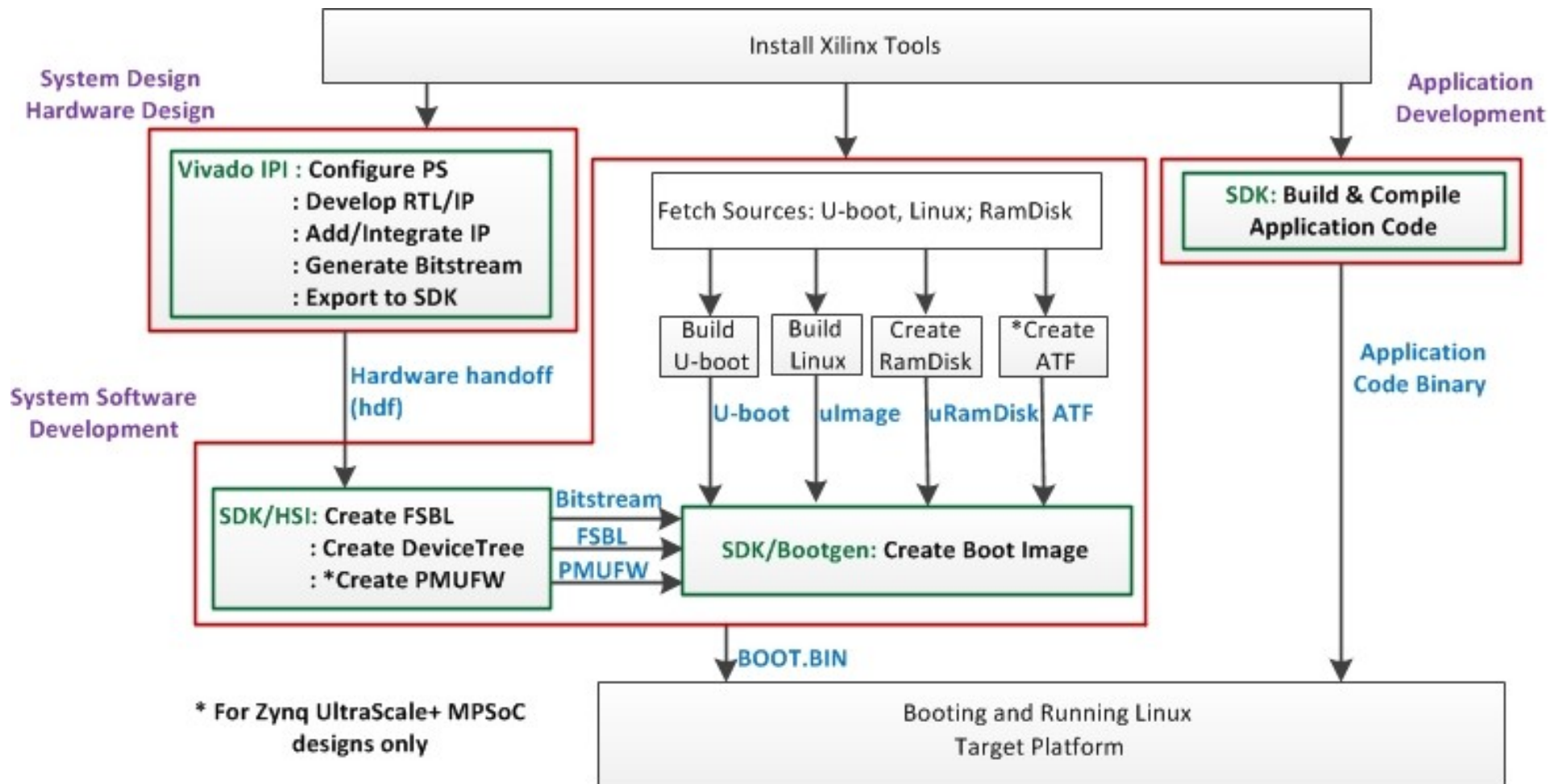


*Running Linux*



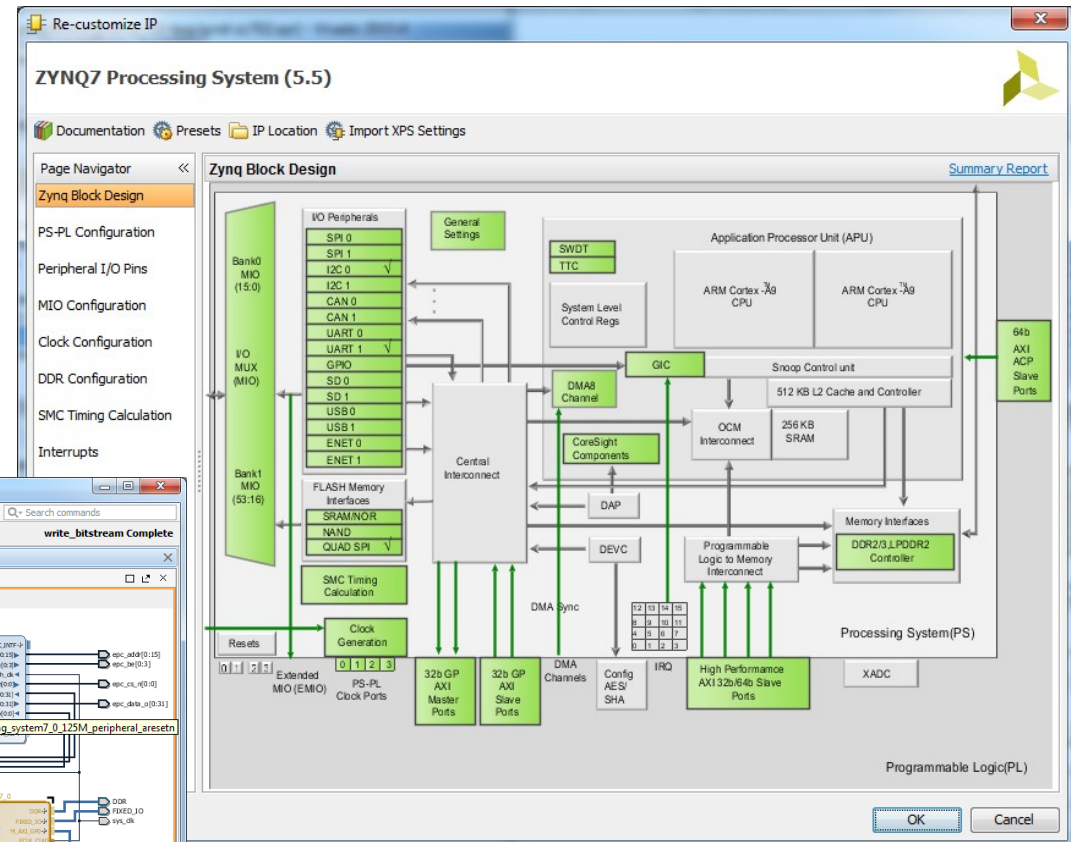
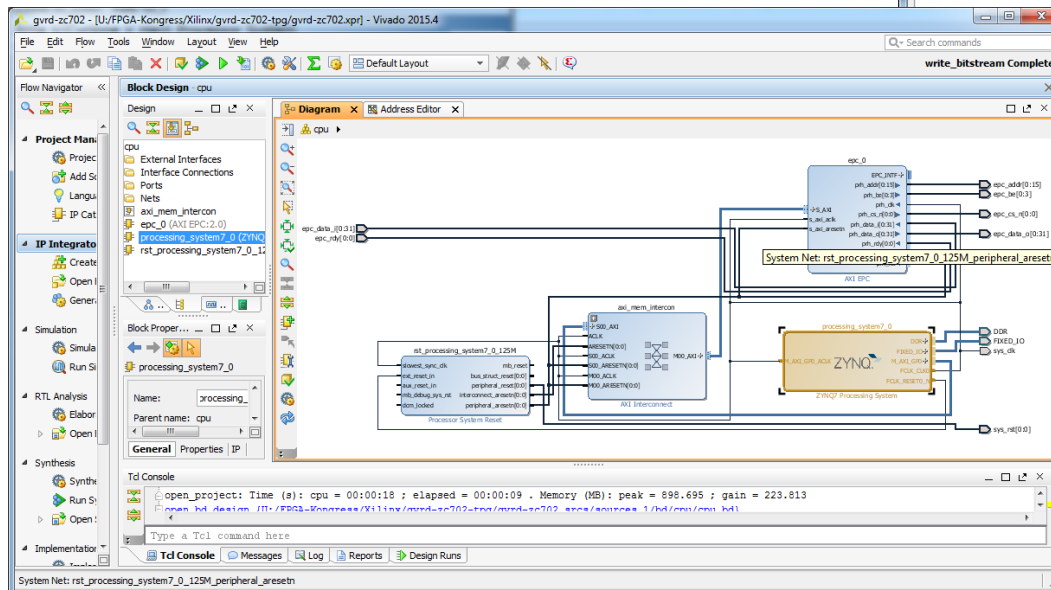


# Xilinx Zynq Design Flow



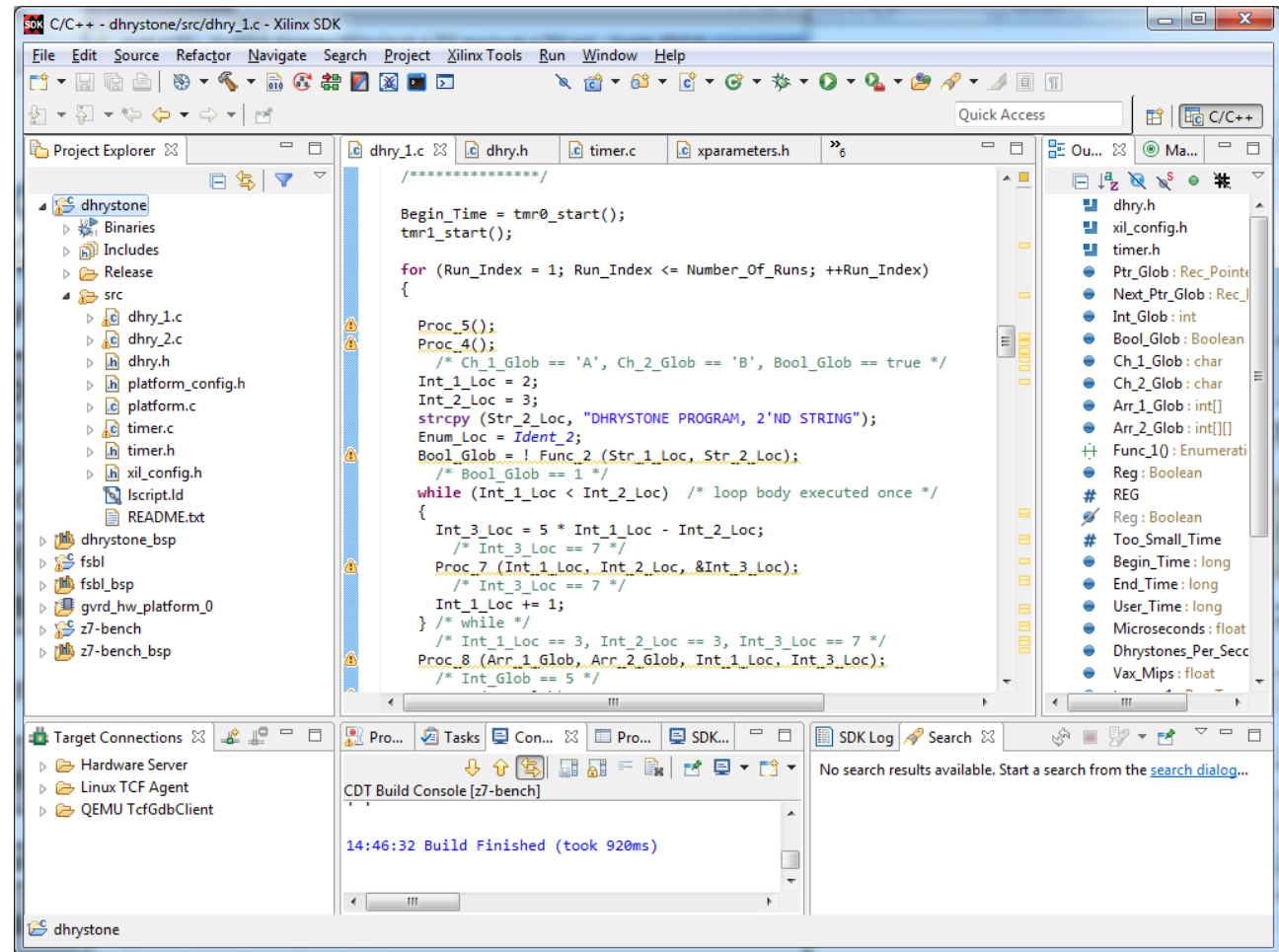
# Zynq System Generation

- HW-Tools:
  - Vivado
  - Vivado IP Integrator



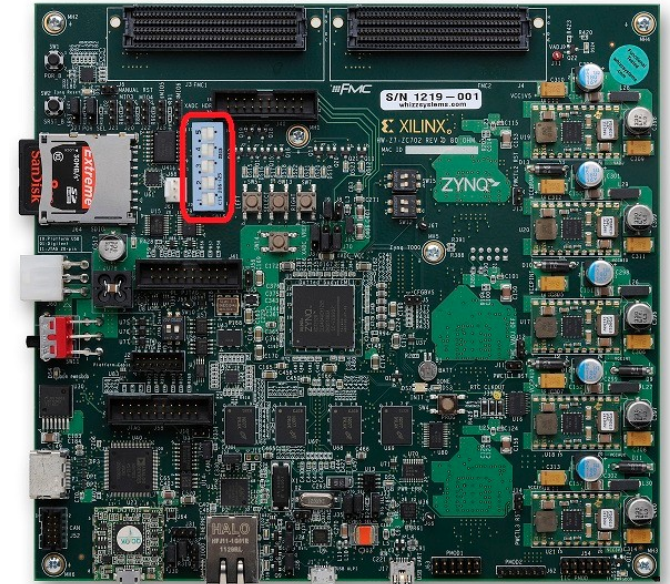
# Zynq SW Development

- Xilinx SDK
- HW Platform
- FSBL
- Application



# Xilinx Zynq Platform

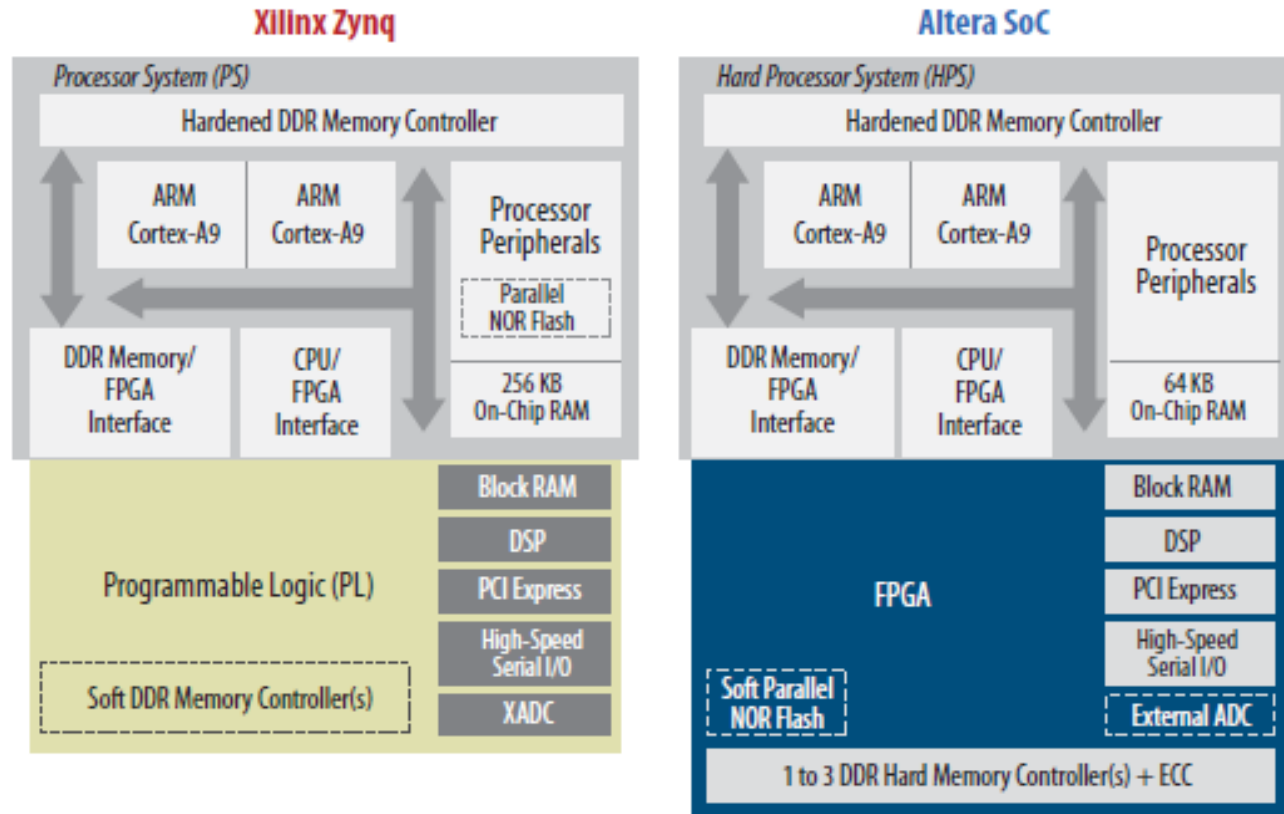
- Xilinx ZC702
  - FPGA: Zynq-7000 XC7Z020-1CLG484C AP SoC
    - 85K logic cells
    - 53,200 LUTs
    - 220 DSP slices
    - Block RAM (Mb): 4.9



# Cyclone V Soc / Xilinx Zynq

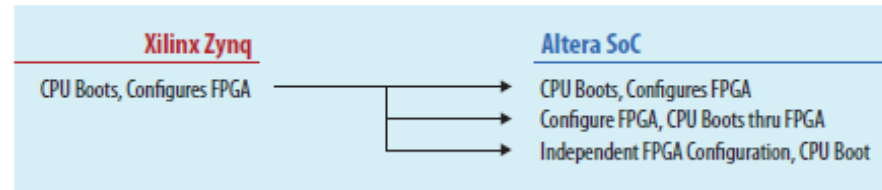
Figure 1. High-Level Comparison of Zynq and Altera SoC Architectures

- High level comparison



- Boot modes

Figure 3. Zynq and Altera SoC Boot and Configuration Modes

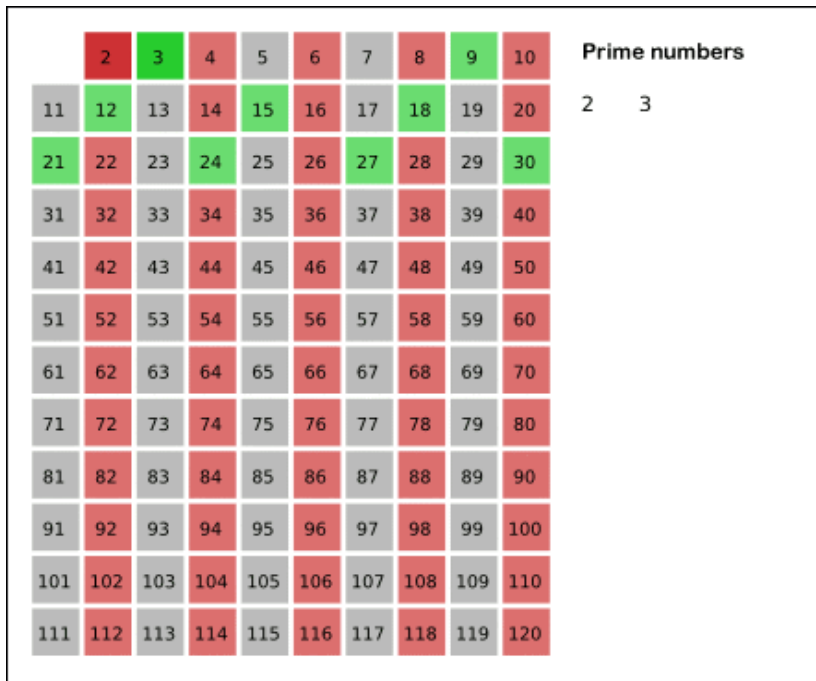


# Benchmarks

- Sieve of Eratosthenes
- Dhrystone

# Sieve of Eratosthenes

- Simple algorithm finding prime numbers up to a given integer
- List of all number from 2, 3, 4, ... to max value N
- Iterative marking as “not prime” of multiples of each prime



# Sieve benchmark results 1/2

CPU	frequency [MHz]	N	duration	time unit
PB8051	48	2,000	608.00	ms
Nios II gen2	100	2,000	692.00	us
MicroBlaze	100	2,000	309.00	us
Cyclone V SoC BM	925	2,000	158.00	us
Zynq BM	666	2,000	6.40	us

CPU	frequency [MHz]	N	duration	time unit
Nios II gen2	100	15,000	5.79	ms
MicroBlaze	100	15,000	1.87	ms
Cyclone V SoC BM	925	15,000	1.20	ms
Zynq BM	666	15,000	26.26	us



# Sieve benchmark results 2/2

CPU	frequency[MHz]	N	duration	time unit
Nios II gen2	100	20,000	Out of memory	
MicroBlaze	100	20,000	2.47	ms
Cyclone V SoC BM	925	200,000	16.89	ms
Cyclone V SoC Linux	925	200,000	6.00	ms
Zynq BM	666	200,000	0.33	ms
Zynq Linux	666	200,000	8.00	ms

CPU	frequency[MHz]	N	duration	time unit
Cyclone V Soc BM	925	2,000,000	177.59	ms
Cyclone V Soc Linux	925	2,000,000	68.00	ms
Zynq BM	666	2,000,000	3.70	ms
Zynq Linux	666	2,000,000	95.00	ms

# Dhrystone 2.1

- 1984 by Reinhold Weicker, Siemens AG
  - First revision in Ada and Pascal
  - Now C version mainly used
- Synthetic performance benchmark
  - Easy-to-use
  - General-purpose (“integer”)
  - 12 different subroutines:
    - Pointer and array access operations
    - Simple arithmetic and logic operations
    - If statements and string operations
- Result: DMIPS(/MHz)
  - **D**hrystone **M**illion **I**nstructions **P**er **S**econd
  - 1 DMIPS = 1757 Dhrystones / s

# Dhrystone benchmark results

CPU	frequency [MHz]	Dhrystone run [us]	Dhrystones / second	DMIPS / second	DMIPS / MHz
Nios II gen2	100	10.660	93,808	53.4	0.533
MicroBlaze	100	9.430	106,044	60.4	0.603
Zynq BM	666	0.324	3,086,419	1,756.6	2.637
Cyclone V SoC BM	925	8.320	120,180	68.4	0.073
Zynq Linux	666	0,482	2,075,980	1181,5	1,774
Cyclone V SoC Linux	925	0.347	2,884,616	1,641.8	1.775
Intel Core i3-4130	3,400	0.035	28,193,634	16,046.5	4.585

The logo for 'sensor to image' features the text in a bold, italicized sans-serif font. A green graphic element, consisting of a curved line on the left and a stepped staircase-like shape on the right, arches over the text.

***sensor to image***

Thanks for your interest and time!

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